METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT NANOSTRUCTURE SPIN LATTICE DEVICES

by

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STATEMENT OF DISSERTATION APPROVAL

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ABSTRACT

This dissertation explored and developed technologies for silicon based spin lattice devices. Spin lattices are artificial electron spin systems with a periodic structure having one to a few electrons at each site. They are expected to have various magnetic and even superconducting properties when structured at an optimal scale with a specific number v of electrons. Silicon turns out to be a very good material choice in realizing spin lattices. A metal-oxide-semiconductor field-effect nanostructure (MOSFENS) device, which is closely related to a MOS transistor but with a nanostructured oxide-semiconductor interface, can define the spin lattices potential at the interface and alter the occupation v with the gate electrode potential to change the magnetic phase. The MOSFENS spin lattices engineering challenge addressed in this work has come from the practical difficulty of process integration in modifying a transistor fabrication process to accommodate the interface patterning requirements.

Two distinct design choices for the fabrication sequences that create the nanostructure have been examined. Patterning the silicon surface before the MOS gate stack layers gives a "nanostructure first" process, and patterning the interface after forming the gate stack gives a "nanostructure last process." Both processes take advantage of a nano-LOCOS (nano-local oxidation of silicon) invention developed in this work. The nano-LOCOS process plays a central role in defining a clean, sharp confining potential for the spin lattice electrons.

The MOSFENS process required a basic transistor fabrication process that can accommodate the nanostructures. The process developed for this purpose has a gate stack with a 15 nm polysilicon gate electrode and a 3 nm thermal gate oxide on a p-type silicon substrate. The measured threshold voltage is 0.25 V. Device processes were examined for either isolating the devices with windows in the field oxide or with mesas defined by the etched trenches filled with oxide.

The nanostructrure patterning processes combined electron beam lithography, reactive ion etching and the nano-LOCOS in a nanostructure last fabrication sequence. The electron beam tool produced holes with diameters down to 10 nm and lattice periods down to 50 nm for defining the spin lattices. The dry etching process was able to transfer the pattern into the polysilicon gate material, and the depth was controlled using the measured etching rate. These dimensions are sufficiently small for spin lattices properties to be important at low temperatures.

Upon combining the NMOS and the nanostructure last processes, MOSFENS spin lattice devices were successfully fabricated. The gates are patterned with lattices having a 50 nm period and 20 nm holes, which is the optimal, targeted ratio of 2.5 for superconductivity. The room temperature current-voltage characteristics of these devices show that the lattice nanostructures significantly reduce the average channel mobility, as expected. However, the essentially unchanged threshold voltage indicates the nano-LOCOS process has given a low-defect nanostructure interface. At room temperature, a change in gate potential of approximately of 18 mV changes the lattice electron occupation from $\nu = 1$ to $\nu = 2$. For these devices, the predicted temperature scale for superconductivity is approximately at 9 K.

I dedicate this dissertation to my wife Jin for her support, patience, and encouragement, and to our beloved daughter Gianna.

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CHAPTER 1

INTRODUCTION

Silicon nanostructures structured at an optimal dimension scale are promising for implementing magnetic and superconducting systems, and such periodic structures have been referred to as spin lattices [1, 2, 3]. We propose a nanostructure that is similar to the MOS (metal-oxide-semiconductor) transistor but with a patterned, undulating oxide-semiconductor interface to serve as a platform for spin lattice applications. The field-effect perpendicular electric filed at the interface is able to modulate and engineer the in-plane two-dimensional electron gas (2DEG) (Fig. 1.1) [2, 4]. This nanostructure is referred to as "metal-oxide-semiconductor field-effect nanostructure (MOSFENS)." One of the great challenges for MOSFENS engineering is the process integration of how to modify an established MOSFET (metal-oxide-semiconductor field-effect transistor) fabrication process to accommodate the interface patterning requirements [5].

As illustrated in Fig. 1.1, the gate-to-substrate perpendicular surface electric field E_s in a MOSFENS device pushes the inversion layer electron gas in the silicon up against a patterned oxide interface. The undulating Si-SiO_2 interface gives a local effective in-plane electric field E_p [2]. Take the average interface plane to be the x plane, with y into the substrate, and describe the surface topography by its height in the y-direction, $h(y)$. For the moment, neglect the different permittivity for silicon and silicon dioxide. Setting the electron potential energy at the lowest h-point to zero, the potential energy along h

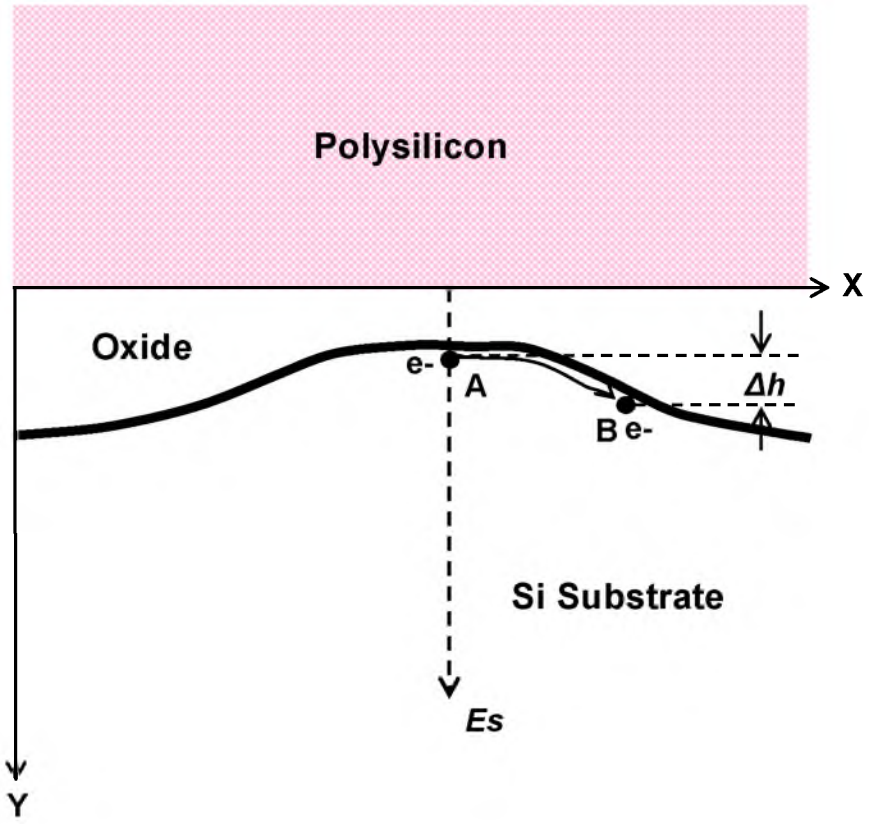

Fig. 1.1: Engineering strongly-coupled electrons by undulating topography at the Si-SiO_2 interface in a MOSFENS: The electron is held tightly to the thinnest portion of the oxide (position A) where the lowest potential resides. The electron has to overcome the perpendicular electrical field E_s to move in a distance of Δh to another location (position B) where the potential is higher.

varies as qhE_s, and the local in-plane effective electric field is:

$$E_p = E_s \nabla h \tag{1.1}$$

Taking E_s = 1 MV/cm, for h = 3 nm, the scale of the effective in-plane electric field over a half-period is about 0.3 MV/cm, a significant fraction of E_s for such a modest perturbation of the Si-SiO_2 interface. The corresponding potential energy increases over a half period to 300 meV. It is important to have a smooth Si-SiO_2 interface and high quality oxide of minimum interface traps and fixed charges to prevent oxide tunneling.

In this chapter, section 1.1 presents the concept of spin lattices and their various magnetic and superconductivity properties related to the electron-per-site filling factor v. Section 1.2 introduces material selection to meet the requirement of spin lattices. Section 1.3 gives the technology challenges in realizing spin lattices by using MOS structures. In section 1.4, the outline of this dissertation is described.

1.1 Spin Lattices

One important application of MOSFENS devices should be to realize spin lattices. Spin lattices are artificial electron spin systems with a periodic structure having one to a few electrons at each site, and the electrons are confined within a small island. Spin lattices can show atom-like behavior, but they have two characteristics that are very different from those of actual atoms. The first characteristic is that the distance between the lattice structures is unchangeable when the electrons are strongly tied to the sites, while the bond length of atoms can be varied. The second characteristic is that the number of electrons at each engineered site can be altered, whereas in atoms this is fixed. Spin lattice structures are not susceptible to lattice deformations; therefore, they can be designed freely without considering potential lattice instabilities [6].

Koskinen and others showed that because of the interplay between electron charge, motion, spin, exchange, and correlation, spin lattices have rich magnetic properties, depending on the lattice constant and the electron number [7]. The electron-per-site filling factor v is defined as the number of electrons bound to each site, and Fig. 1.2 depicts anti-dot single occupation square spin lattices with $v = 1$. Theorems by Lieb predict that $v = 1$ gives an anti-ferromagnetic phase, and $v = 3$ a ferromagnetic phase, while $v = 2$ and 4 result in quantum insulating phases [6].

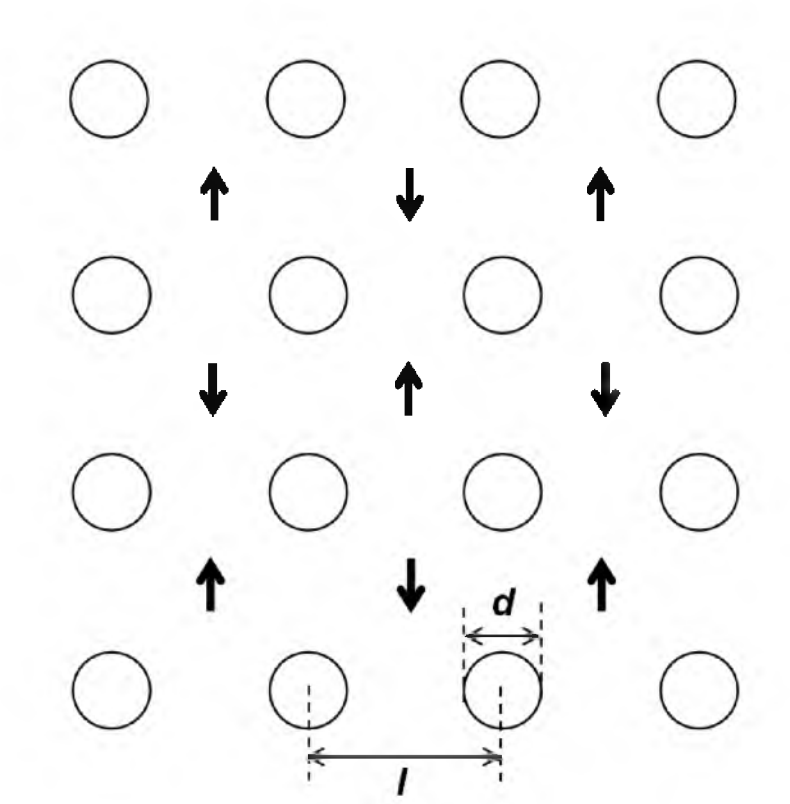

Fig. 1.2: The diagram shows single occupation anti-dot square spin lattices. The spin lattices are occupied by the electrons, which are represented in arrows with a spin direction in parallel. The circles represent the holes separating the sites with the size of *d* and the period in *l*.

One of the most fascinating potential applications of spin lattices engineering is high temperature (high-T_c) superconductivity [8, 9, 10, 11]. Although the energy scales or the transition temperature is smaller than the conventional CuO_2 high-T_c superconductors [12], superconductivity in spin lattices might be possible. Single-electron band calculations also suggest that an anti-dot geometry of spin lattices with optimal dimensions should have a ratio between the lattice period *l* and the hole size *d* of 2.5. For instance, for a hole size at 10 nm and lattice period at 25 nm, the gap energy scale estimation is 19 K. For a hole size at 20 nm and lattice period at 50 nm, the gap energy scale should be 7 K [2].

Spin lattices may be adapted for use in a number of device applications, including spintronics, fast processing and high-density bit storage, magnetic field sensors, and switches for logic circuits, etc.

Importantly, the theoretical predictions for the magnetic phases rely on particular assumptions, and approximations that are often in disagreement; and the underlying models are notoriously hard to solve. Working MOSFENS spin lattice devices should help to set some boundaries for choosing between theoretical approaches, in addition to any technological benefits from these devices.

1.2 Material Selection for Spin Lattices

There have been several efforts undertaken to realize spin lattices based on different materials, like carbon networks [13, 14], graphite ribbon [15], As [16], GaAs atomic wires [17, 18], and InAs lattices [19]. However, there is no clear evidence so far of the observation of ferromagnetism. Because it is difficult to form the lattices using these materials and the lattice distortion would destabilize ferromagnetism [20].

Silicon turns out to be a very good material choice in realizing spin lattices because of a good compromise between the conflicting goals of a small dielectric constant and a small effective mass (see section 2.1) [2]. With their gate electrodes patterned with holes at the optimal scale and period, MOSFENS devices provide a platform for realizing spin lattices with advantages. The first advantage is that the electron-per-site filling factor ν and accordingly the magnetic phases can be controlled by changing the gate potential. The second advantage is that the Si-SiO_2 interface gives a smooth confinement barrier for defining the spin lattices. The properties of Si-SiO_2 interface are well studied. Furthermore, effective approaches to minimize the interface traps are available for use

(see Appendix A) as it is critical for MOSFENS spin lattice devices to have a significantly lower number of interface traps compared to the overall spin lattice sites [2]. The third advantage is that there is an immense and still growing semiconductor technology base for fine-scale structures like MOSFENS.

1.3 MOS Spin Lattices Technology Challenges

The central MOSFENS spin lattices engineering challenges come from the great difficulties in modifying an established transistor fabrication process to accommodate the interface patterning requirements [5]. These modifications make it difficult to fabricate MOSFENS spin lattice devices in a foundry service. To better understand this, it is beneficial to briefly introduce the advanced processes used in contemporary deep sub-micron MOSFET structures.

Because direct tunneling increases exponentially with decreasing oxide thickness, it may not be feasible to use SiO_2 with thickness smaller than 1.5 nm. A wide variety of high-k materials have been studied as the alternative to SiO_2 (k = 3.9) for deep sub-micron MOSFET, like Ta_2O_5 (k = 23) [21], Al_2O_3 (k = 10) [22], ZrO_2 (k = 23) [23] and HfO_2 (k = 20) [24]. The ideal gate dielectric stack has an interface consisting of a few atomic layers of Si-O (and possibly nitride), containing a pseudo-binary oxide. This oxide layer could preserve the critical high quality characteristics of the SiO_2 interface while providing a higher k value. Then a different, higher-k material could be used on top of this interfacial layer.

The replacement gate process architecture avoids the problems of work function material stability seen in the gate first architecture. The original deposited polysilicon will be removed and be replaced by metal gate (like Al alloys), which has much lower

resistivity [25].

Self-aligned process does not require any additional masking steps, and it forms silicide (like $TiSi_2$, NiSi or $CoSi_2$) on the source and the drain regions only to achieve low resistivity [26]. On the traditional gate first process, the silicide is also formed at the same time on the polysilicon gate.

Shallow trench isolation (STI) isolates the transistors by the oxide buried in deep trenches, and it provides better isolation between the devices compared to the conventional LOCOS (local oxidation of silicon) by minimizing the channel current leakage under the field oxide. Meanwhile, STI offers superior latch-up immunity, smaller channel-width encroachment and much better planarity [27].

Strained silicon is a layer of silicon in which the silicon atoms are stretched beyond their normal interatomic distance. This can be accomplished by putting the layer of silicon over a substrate of silicon germanium (SiGe). In this way, higher mobility in the channel consequently leads to a larger channel current [28].

Fig. 1.3 shows a cross-section view of a MOSFENS spin lattice device. It uses ALD (atomic layer deposition) technique to grow a SiO_2-SiN stack of gate dielectric (see section 7.3), and the mesa isolation (see section 3.3) using STI technologies. Ultra-thin gate oxide instead of high-*k* materials is used for MOSFENS spin lattice devices, because the ultra-thin oxide provides a stronger perpendicular electric field at the interface. In addition, the thin oxidation technique is also applied to the nano-LOCOS (nano-local oxidation of silicon) process, which will be introduced in section 3.2.

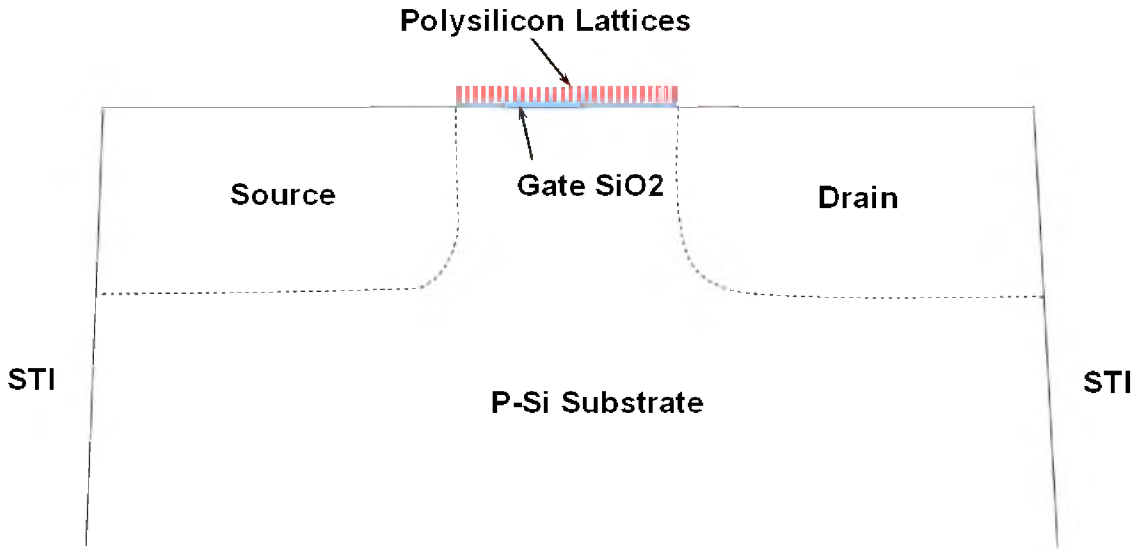

Fig. 1.3: Schematic cross-section view of a MOSFENS spin lattice device, which has 3 nm gate oxide and 15 nm gate polysilicon. The gate is patterned with the lattice holes.

1.4 Outline of This Dissertation

Chapter 2 provides an overview of two distinct design choices for the fabrication sequences of the nanostructure formation. Patterning the silicon surface before the MOS gate stack layers gives a "nanostructure first" process, and patterning the interface after forming the gate stack gives a "nanostructure last" process. Both processes take advantage of a nano-LOCOS invention developed in this work. The nano-LOCOS process plays a central role in defining a confining potential for the spin lattice electrons.

The MOSFENS process requires a basic transistor fabrication process that can accommodate the nanostructures. In Chapter 3, the developments, the fabrication process flow and the characterizations of an NMOS (*n*-type metal-oxide-semiconductor) process are presented. In addition, the processes are examined for either isolating the devices with the windows in the field oxide or with the mesas defined by the etched trenches filled with oxide.

Chapter 4 introduces the nanostructrure patterning processes that combine the electron beam lithography (EBL), the reactive ion etching (RIE) and the nano-LOCOS in a nanostructure last fabrication sequence. The electron beam tool gives holes with diameters down to 20 nm and lattice periods down to 50 nm for defining the spin lattices. The RIE process is able to transfer the pattern into the polysilicon gate material. These dimensions are sufficiently small for the spin lattices properties to be prominent at low temperatures.

Upon combining the NMOS and the nanostructure last processes, MOSEFENS spin lattice devices were successfully fabricated. Chapter 5 lists the fabrication process flow of MOSFENS spin lattice devices and along with the characterization results.

Chapter 6 is devoted to the summary, the future tasks and the recommendations for the development of next generation MOSFENS devices.

CHAPTER 2

TECHNICAL BACKGROUND

In this chapter, the technical background and the models are presented. In section 2.1, a method based on a strong coupling electrons system is used to identify good materials for the spin lattice implementation. In section 2.2, a MOS model used to calculate the 2DEG concentration at the Si-SiO_2 interface is introduced. In section 2.3, the 2DEG concentration based on various lattice length scales is calculated for comparison with the typical value of the fixed oxide charge concentration N_f.

2.1 Spin Lattices Material Selection

Strong coupling requirement for the spin lattices asks the semiconductor material to balance between the kinetic energy and the charging energy [2]. The kinetic energy E_t can be calculated by the lowest confinement energy of a carrier in that material to a sphere of radius a,

$$E_t = \frac{\pi^2 \hbar^2}{2m^* a^2} \tag{2.1}$$

with m^* the effective mass and $\hbar$ Planck's constant.

The charging energy E_U for a spherical region radius a can be obtained as:

$$E_U = \frac{q^2}{4\pi\varepsilon a} \tag{2.2}$$

with q the elementary charge and ε the permittivity. These energies balance at the strong coupling [29] length scale:

$$a^* = \frac{2\pi^3 \hbar^2 \varepsilon}{q^2 m^*} \tag{2.3}$$

For an electron of mass m_0, and permittivity ε_0 in vacuum, the strong coupling length a^* = 261 pm, which is about five times of the Bohr radius. For spin lattices, a larger length scale is easier to fabricate and a larger strong coupling energy gives higher operation temperature.

Fig. 2.1 plots the strong coupling energies of several materials versus their strong-coupling length scales reproduced from Mark's calculation [2]. III-V semiconductor materials have small effective masses, but small masses generally come with larger permittivity and consequently, smaller strong coupling energies E^*. For GaAs, of which electron effective mass m^*_n = 0.067 m_0 and ε_r = 13.1, the scales are a^*_{GaAs} = 51.1 nm and E^*_{GaAs} = 2.15 meV. As another example, InAs, of which m^*_n = 0.023 m_0 and ε_r = 14.6, has a larger a^*_{InAs} = 166 nm but even smaller E^*_{InAs} = 0.59 meV. For n-type Si, taking m^*_t = 0.19 m_0 and ε_r = 10.9, it has E^*_{Si} = 8.8 meV and a^*_{Si} = 15.0 nm. This energy corresponds with the thermal energy scale for liquid nitrogen at 6.6 meV, and the length scale lies well within the reach of present fine patterning technologies including EBL. Overall, this analysis suggests that silicon is an ideal candidate to realize strong coupling spin lattice systems, since it has both a large practical E^* and a^* giving rise to spin lattices operating within reach of liquid nitrogen temperature.

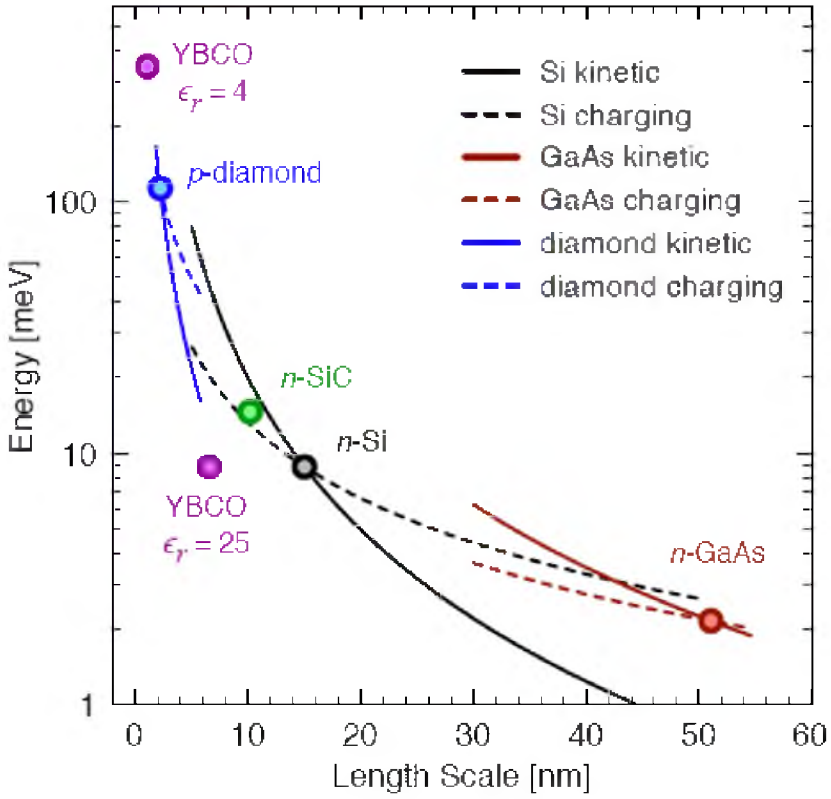

Fig. 2.1: The strong-coupling energy scale plotted versus length scale for several candidate spin lattices materials. Solid lines plot the kinetic energy Et and dashed lines the charging energy E_U dependence on length scale for *p*-diamond, *n*-Si, and *n*-GaAs, with line colors corresponding to the a point for each material. The two points for YBCO (yttrium barium copper oxide) [30] assume two values for the permittivity [2].

2.2 MOS Models

A positive gate voltage will form an inversion layer of 2DEG at the Si-SiO_2 interface on *p*-type material MOS structures. For a MOSFENS spin lattice device with sites the size of a, the occupation of the lattice sites is approximately $n_s a^2$, where n_s is the 2DEG concentration for a given gate bias potential. Therefore, when the inversion layer of 2DEG begins to form at the Si-SiO_2 interface, the gate potential V_g equals to the threshold potential V_t, and it can be calculated as:

$$V_g = V_t = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_{Si} q N_a (2\psi_B + V_{bs})}}{C_{ox}} \tag{2.4}$$

where N_a is substrate doping concentration N_a.

The flat-band voltage V_{fb} is taken to be the work function difference between the gate polysilicon and semiconductor, and the oxide has a capacitance per area of $C_{ox} = \varepsilon_{ox}/t_{ox}$, with ε_{ox} and t_{ox} the oxide permittivity and thickness. The bulk potential is defined as $\psi_B = V_{th} ln(N_a/n_i)$, with n_i the silicon intrinsic carrier concentration, and $V_{th} = k_B T/q$ the thermal potential, with k_B Boltzmann's constant. The body bias potential V_{bs}, applied from the substrate to the inversion layer, can shift the threshold voltage. Above threshold, the two-dimensional inversion layer electron concentration is approximately [34]:

$$n_s = \frac{C_{ox}}{q}(V_g - V_{t)} \tag{2.5}$$

Below threshold, the 2DEG concentration varies exponentially with the gate potential as [31]:

$$n_s = \frac{V_{th} N_a}{E_s} e^{\frac{(V_g - V_t)}{m V_{th}}} \tag{2.6}$$

where m is the body effect coefficient.

The surface electric field at the Si-SiO_2 interface is:

$$E_s = \sqrt{\frac{2qN_a(2\psi_B + V_{bs})}{\varepsilon_{Si}}} \tag{2.7}$$

This electric field has a characteristic scale of 1 MV/cm in silicon based MOS. Together with the gate potential, the back gate potential V_{bs} provides a means to independently vary the inversion layer concentration as well as the surface electric field E_s in the semiconductor at the interface.

2.3 Strong Coupling Length in Silicon MOS

According to Mark's calculation [2], Fig. 2.2 plots representative ranges of the 2DEG concentration n_s versus the gate potential V_g for p-type substrate at 77 K. Take the substrate doping concentration N_a from 1×10^{15} cm^{-3} to 2×10^{18} cm^{-3}, and with gate oxide thickness t_{ox} = 3 nm giving threshold voltages of 40 mV to 800 mV. The gray dotted line represents the typical value at 10^{10} cm^{-2} of the fixed oxide charge concentration N_f for contemporary advanced MOSFETs [32]. The right Y axis in Fig. 2.2 gives the length scale a estimation based on n_s, and $a \approx 1/\sqrt{\varepsilon_{Si}}$. For the silicon strong-coupling length scale of a^*_{Si} = 15.0 nm mentioned in section 2.1, it corresponds approximately to ns at 4×10^{11}cm^{-2} (Table 2.1) for single electron occupation spin lattices.

In summary, silicon is found to be a very good material in realizing spin lattices due to its considerably high strong coupling energy with length scale that are within the reach of contemporary technologies. By comparing the 2DEG concentration, which is calculated by a silicon based MOS model, a guide is given to select the appropriate length scale in order to have significantly higher electrons at the Si-SiO_2 interface than the fixed oxide charge concentration N_f.

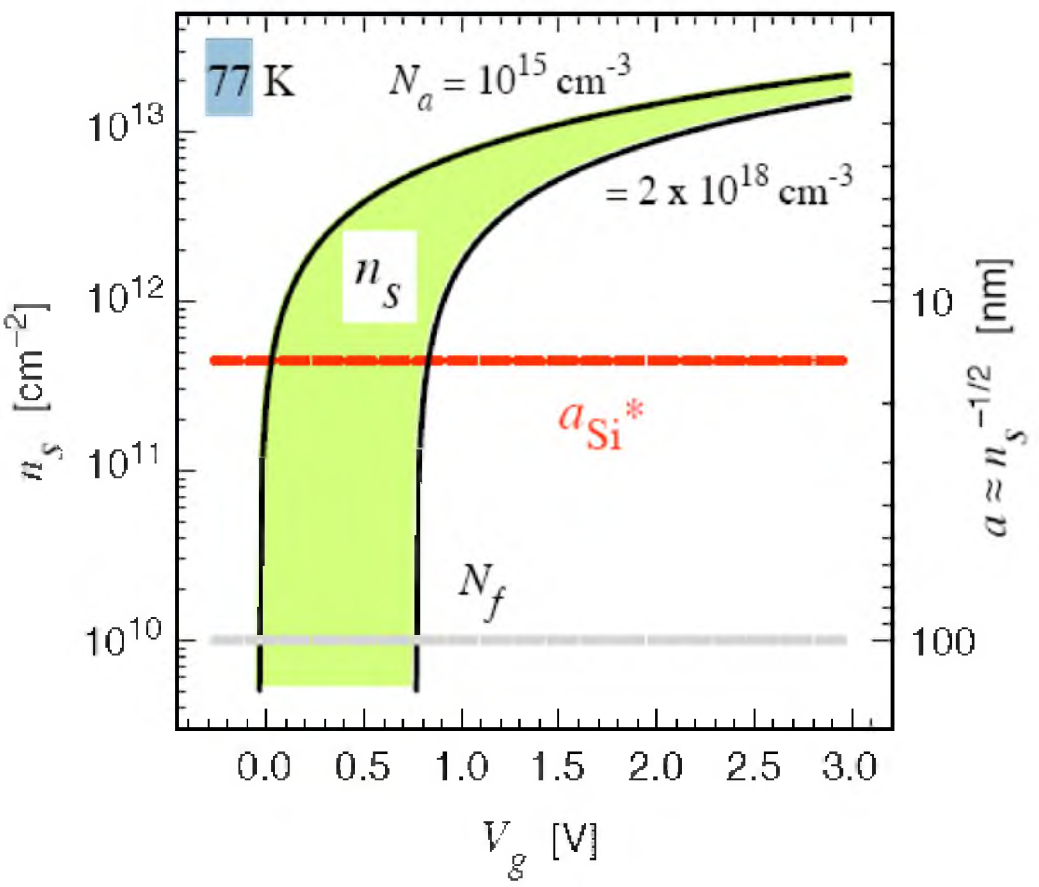

Fig. 2.2: Inversion layer 2DEG density versus gate voltage at 77 K spanned by two doping densities. A gray dashed line plots an estimate for the fixed interface charge density N_f. The right axis scale gives a corresponding length scale estimate per single electron of $a \approx 1/\sqrt{\varepsilon_{Si}}$, with the strong coupling length scale for silicon a^*_{Si} plotted with a red dashed line [2].

Table 2.1: Two-dimensional electron gas densities in a MOSFET that correspond to those needed to achieve one-electron-per-site for a given lattice scale a.

Lattice Length Scale a (nm)	2DEG Density n_s (cm^{-2})
1000	10^8
100	10^9
50	4×10^{10}
15	4×10^{10}
10	10^{12}

CHAPTER 3

FABRICATION PROCESS AND DEVICE DESIGN

In this chapter, two distinct choices of forming nanostructures are introduced. Both processes take advantage of a nano-LOCOS invention developed in this work, described in section 3.2. Nano-LOCOS process provides a realistic processing route to engineer and manipulate the profile of the electrons at the Si-SiO_2 interface. In section 3.3, two approaches of devices isolation are compared and discussed.

3.1 Nanostructure First and Nanostructure Last

Our implementation of MOSFENS uses an NMOS transistor structure with patterned lattices at the Si-SiO_2 interface to connect the inversion layer electrons. A potential applied to the patterned gate electrode changes the concentration of the 2DEG. There are two choices to form the nanostructures, either before the gate stack formation (the nanostructure first) or after the gate stack formation (the nanostructure last). As schematically indicated in Fig. 3.1, for both designs, the hole size is denoted as d while the period is denoted as l, and the gate electrode is taken to be highly-doped n-type polysilicon. The nanostructure last design has the contact holes vertically etched though the thin polysilicon gate and the initial gate oxide, and subsequently, an oxidation step is used to form smooth interface, with the resulting holes extending a depth of a few

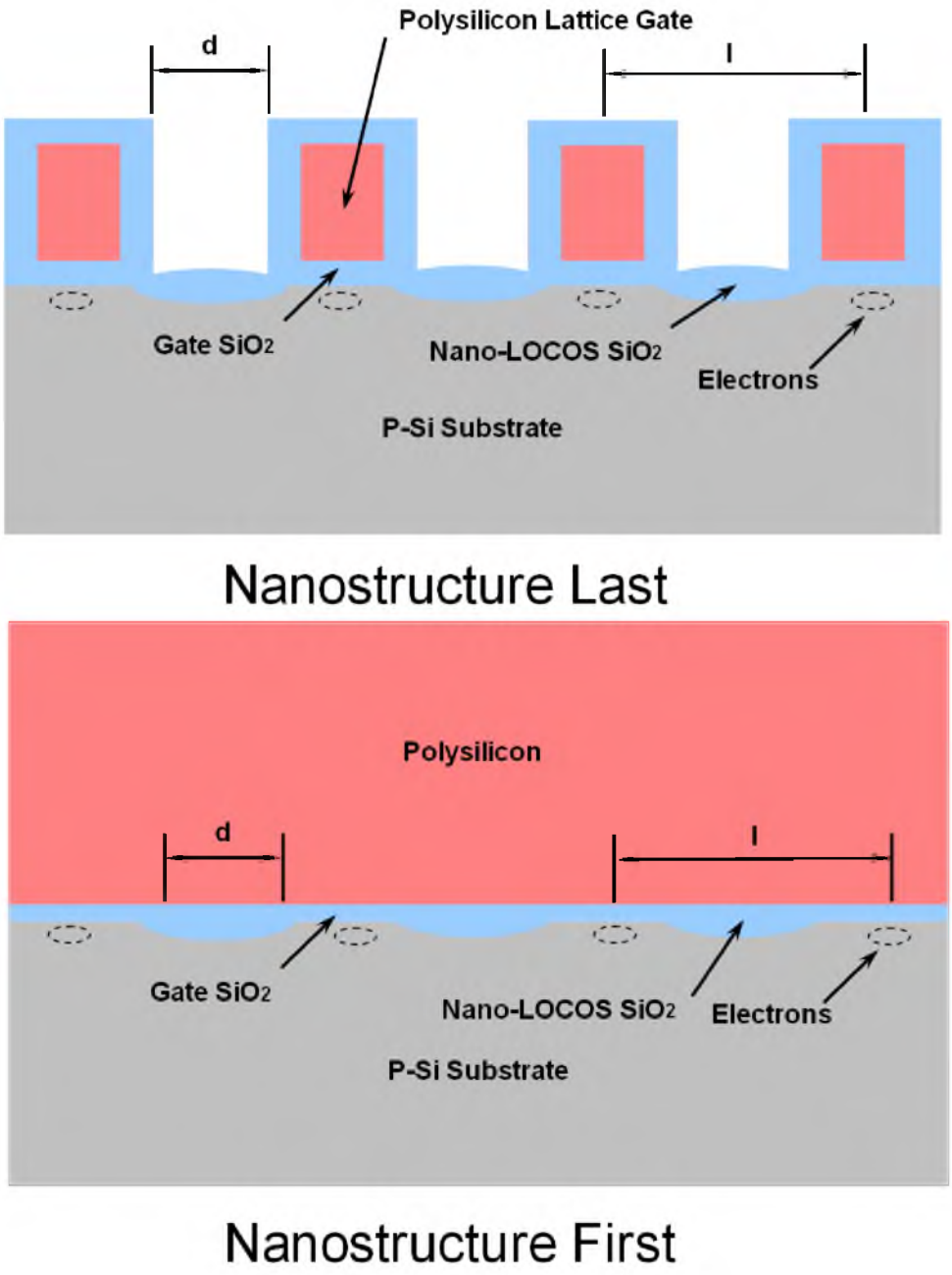

Fig. 3.1: Cross-sections of the nanostructure last design and the nanostructure first design with the hole size = *d* and the period = *l*.

nanometers into the silicon body through the inversion layer region. The nanostructure first design has the oxide obliquely extending into the silicon surface before the gate oxide formation and the lateral undulations combined with the perpendicular electric field confine the electrons near the thinnest oxide regions.

3.2 Nano-LOCOS

Whether forming the nanostructures prior to or after the gate structure formation, both the nanostructure last and the nanostructure first architectures have an undulating Si-SiO_2 interface to confine the electrons to the sites by a perpendicular electrical field. This undulating interface is formed by the nano-LOCOS process, which was invented and developed in this work. The nano-LOCOS process plays a central role in defining a clean, sharp confining potential for the spin lattice electrons, and it grows a 3 nm oxide isolation at the open areas between the nanostructures. After oxidation, POA (post-oxidation annealing) in nitrogen is carried out to minimize the traps and the fixed charges at the Si-SiO_2 interface since it is essential to control the concentration of those traps and charges well below the number of the electrons bound to the sites. This process is very similar to the conventional LOCOS process [33], but it is implemented on a much smaller nanometers scale. Meanwhile, a thin gate oxide is desired to achieve a strong perpendicular electric field E_s [34], and a thin polysilicon layer is required to keep a low aspect ratio during the polysilicon RIE.

3.3 Window Isolation and Mesa Isolation

Two approaches for the isolation between the transistors are pursued in this work (Fig. 3.2). The first one is named "window isolation," and the devices are isolated by the

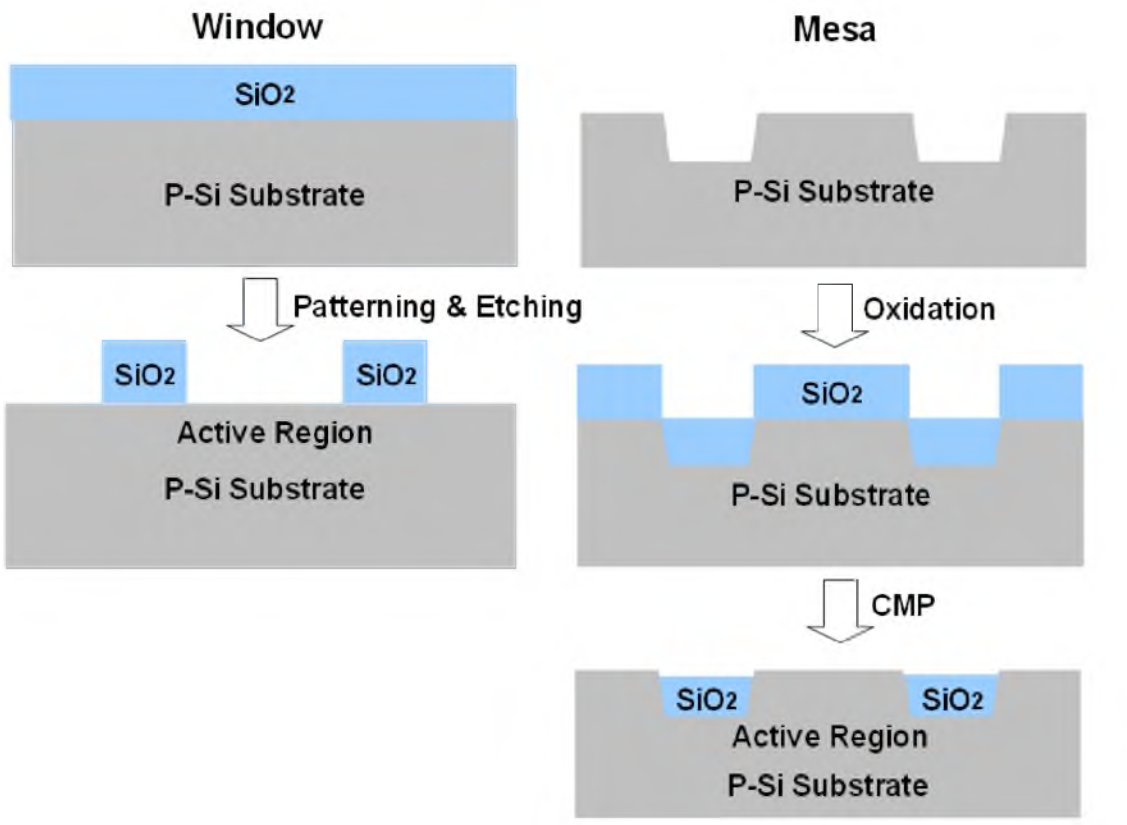

Fig. 3.2: Formation of the window isolation and the mesa isolation. The active region of the window isolation is lower than the oxide, while the active region of the mesa isolation is higher than the oxide in the trench.

patterned field oxide that is grown above the substrate, so the field oxide is higher than the active regions. The second one is referred to as "mesa isolation," and the devices are isolated by the oxide filled in the trenches that are etched into the substrate, so the trench oxide is lower than the active regions.

For the window isolation, the wafer is coated with the photoresist, and the photoresist covers the steps between the active regions and the isolation regions; thus, the photoresist is thicker at the corners of the active regions. It is anticipated that this thicker photoresist area could be subjected to under-exposure due to the DOF (depth of focus) limit of lithography, and the holes would not be opened all the way to the polysilicon gate

beneath. After the polysilicon RIE, the active regions close to the corner will not have the holes open, and consequently the channel current will be shorted by this area of much smaller resistivity (Fig. 3.3). For the mesa isolation, the photoresist thickness inside the active regions is uniform since all the active regions are elevated above the trenches filled with oxide (Fig. 3.3); thus, the under-exposure and shortage issue could be circumvented.

It was decided to use EBL instead of optical lithography for MOSFENS spin lattice devices, and it was demonstrated that this hypothetical issue becomes invalid since the EBL system has much bigger DOF compared to the conventional optical lithography systems [35], and the step height of the window isolation (~300 nm) is well within the DOF range.

In summary, the nano-LOCOS process is designed to use the selective oxidation technique to grow thin oxide between the nanostructures. The nanostructures can be formed either before or after the polysilicon gate formation, and there are two device options: the window isolation and the mesa isolation. All these designs will be applied to the device fabrication in the following chapters.

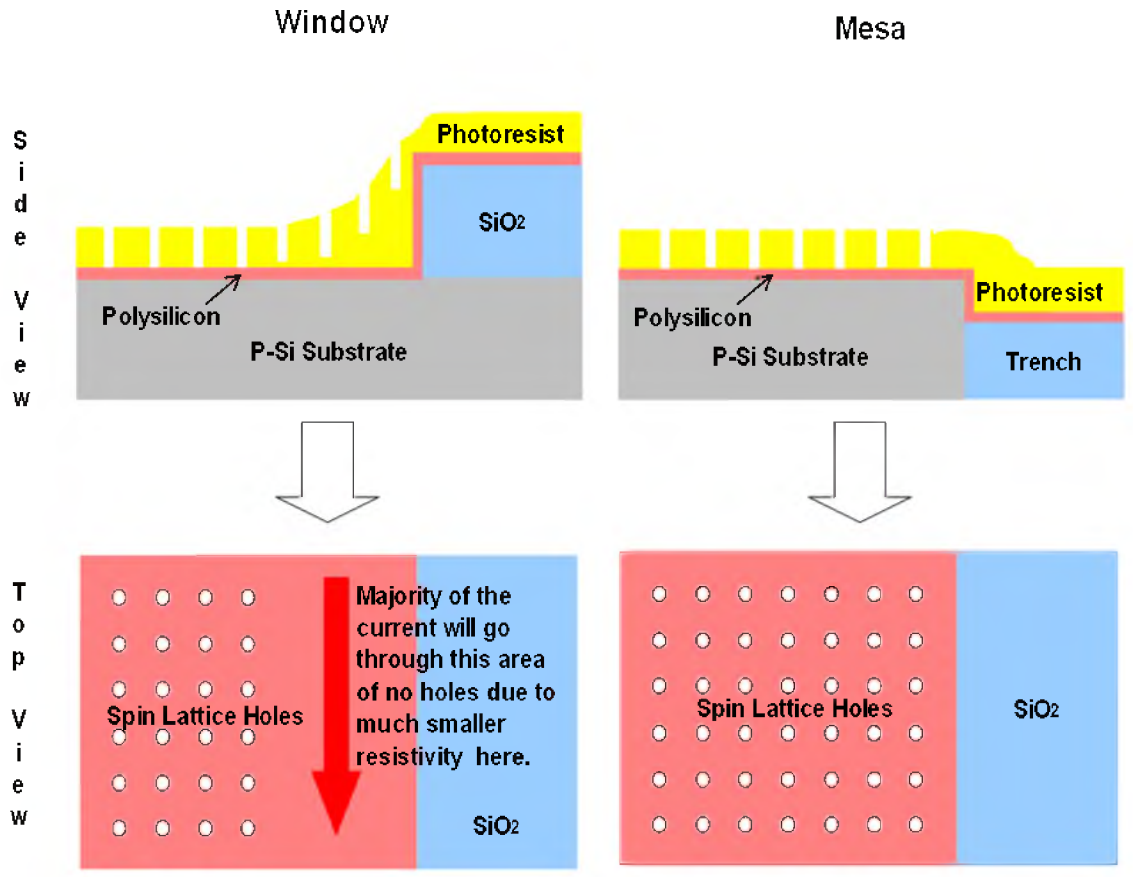

Fig. 3.3: The step height between the active regions and the isolation regions causes underexposure, and consequently, current shortage for the window isolation but not for the mesa isolation.

CHAPTER 4

NMOS PROCESS DEVELOPMENT

The MOSFENS process required a basic transistor fabrication process that could accommodate the nanostructures. In this chapter, as the foundation of MOSFENS devices fabrication, an NMOS process is introduced along with its development, fabrication process flow and characterization results. In section 4.1, the mask design and the layout are introduced, followed by a step-by-step process flow and the characterization results of NMOS processes with the window isolation and the mesa isolation approaches in section 4.2 and 4.3, respectively. In section 4.4, the experimental result of the compatibility between the thin polysilicon and the nano-LOCOS process is presented and discussed.

Engineering the Si-SiO_2 interface topography requires several modifications to the standard MOSFET gate stack in order to implement MOSFENS devices. In a typical NMOS process, the gate oxide is deposited on the silicon substrate where the channel is to be formed, and then the POA is carried out to minimize the traps and the fix charges at the interface. The gate stack continues with a doped polysilicon film and then a silicide layer. These layers are patterned to define the gate features, which are later used as the mask for the self-aligned ion implantation for the source and drain doping.

4.1 Mask Layout

The mask is designed to have eight rows by eight columns, a total sixty four die on a four inch wafer. Each die contains sixteen transistors with the different gate width, and

along with the testing structures of resistivity, contacts and magnetism (Fig. 4.1).

The mask includes five levels. Level one is to define the source and the drain area, and level two is to define the polysilicon gate. Level three is to form the first contact holes on the substrate which will be etched to go through the SOG (spin on glass) layer and the field oxide underneath. Level four is to form the second contact holes on the sources, the drains and the polysilicon gates. Finally, level five is to define the aluminum interconnections and the contact pads.

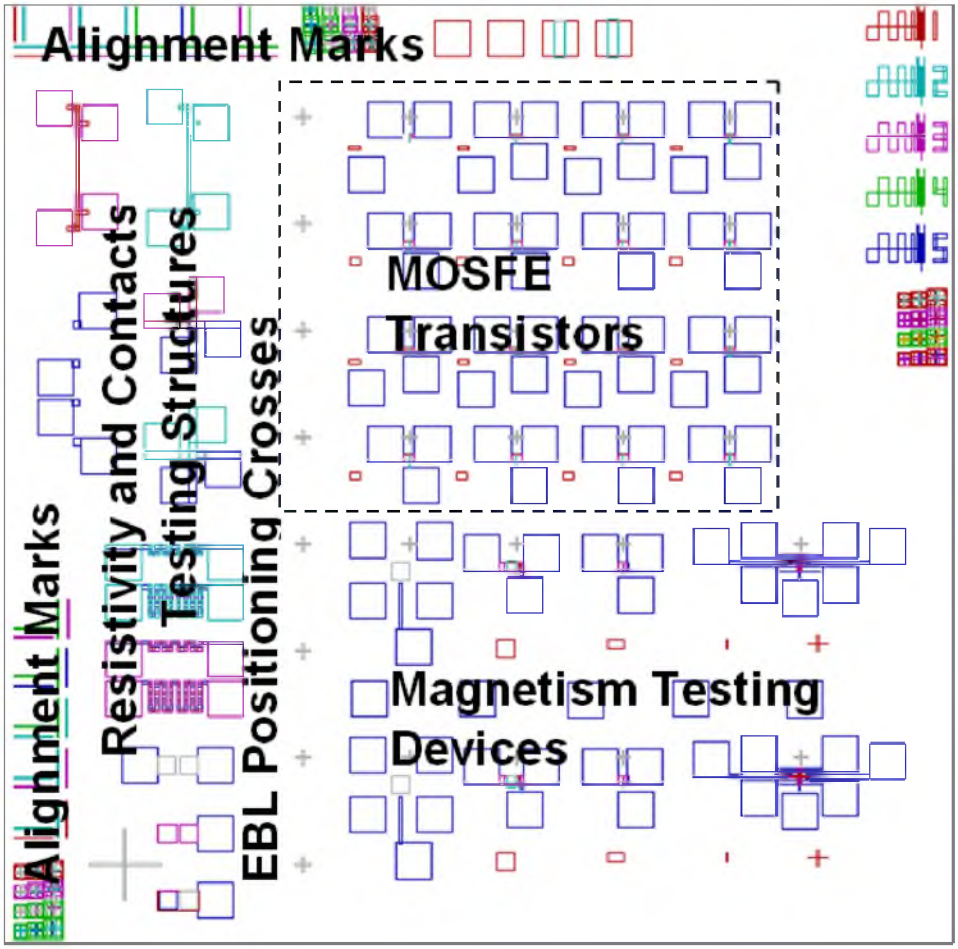

Fig. 4.1: Mask layout of a die

4.2 NMOS Window Isolation Process Flow and Characterization

In this section, the process flow of the NMOS window isolation is presented followed by the characterization results.

4.2.1 NMOS Window Isolation Process Flow

The process steps of the NMOS window isolation for four inch wafers are described step-by-step below. Some important changes made for the migration from two inch wafers are also introduced and discussed.

Step 1 is wafer start. Four inch p type CZ (Czochralski) silicon substrates with boron dopants and <100> crystal orientation were used. The resistivity of the substrates is between 1 to 5 Ω-cm.

Step 2 is field oxide growth. A 370 nm field oxide is thermally grown in a lateral oxidation furnace at 1000°C for 70 minutes by using the wet oxidation technique.

Step 3 is mask one lithography. The purpose of this step is to define the active regions and the nonactive regions. For the window isolation, the active regions will be selectively exposed without the photoresist protection. A negative photoresist is used, and Appendix B details the process steps.

Step 4 is BOE (buffered oxide etchant) etching. The wafer is dipped in 1:6 BOE agent in a wet bench at room temperature for 6 minutes to remove the field oxide at the opened active regions. The etching rate is approximately 92 nm per minute at room temperature. After the BOE etching, the active regions are measured for the oxide thickness on an optical thickness measurement system to make sure there are no oxide

residuals. It is critical to make sure there is no oxide left in the open active regions. Since any oxide residuals will be added to the gate oxide, which will cause an increase in the overall gate oxide thickness, and consequently shifts the actual device performance. Since it is impossible for the microscopic inspection to discover such subtle oxide residuals in nanometers scale, sufficient over-etching and the optical thickness measurement are applied to make sure the oxide has been completely removed. The photoresist is then stripped in acetone and IPA (isopropyl alcohol).

Step 5 is DHF etching. The wafer is dipped in 1:104 DHF (diluted hydrofluoric acid) at room temperature for 3 minutes prior to the gate oxidation to remove the native oxide. It is known that a thin native oxide will grow within a matter of seconds upon exposure to an oxygen-containing ambient or an oxidizing solution. The etching rate of 1:104 DHF at room temperature for 1000 °C grown wet oxide is approximately 3.9 nm per minute.

Step 6 is gate oxide growth and annealing. A 3 nm gate oxide is grown in a lateral oxidation furnace at 800 °C for 8 minutes by using the dry oxidation technique. After the oxidation, the furnace is ramped up to 1050 °C in ambient nitrogen, and stays at 1050 °C for 10 minutes to anneal the fixed oxide charges at the Si-SiO_2 interface (see section 4.3 for the details).

Step 7 is polysilicon deposition. A 40 nm polysilicon film is deposited at 630 °C with a slow deposition rate around 4 nm per minute in a lateral LPCVD (low pressure chemical vapor deposition) furnace (see section 5.2 for the details). The polysilicon thickness will be later reduced to 15 nm after the phosphorous doping.

Step 8 is mask two lithography. The purpose of this step is to pattern the gates. A positive photoresist is used, and Appendix B details the process steps. Mask two has

transistors with a gate width of 2 μm, 3 μm and 5 μm. For small features like 2 μm, the exposure time needs to be short enough (2.5 seconds) to ensure the features can be transferred successfully.

Step 9 is DHF etching. Once the wafer has completed the polysilicon deposition, it is exposed to the ambient, and the native oxide starts to grow on the surface of the polysilicon. For the polysilicon etching recipe with high selectivity to the oxide, the unevenly grown native oxide on the surface leads to poor uniformity during the polysilicon etching. Modern RIE systems have a pre-clean chamber to remove the native oxide before etching the polysilicon in another chamber. However, this function is not available for the LAM490 system in the Nanofab at The University of Utah; therefore, DHF is used instead to remove the native oxide. The wafer is dipped in 1:104 DHF at room temperature for 3 minutes. With an etching rate of the wet oxide at 3.9 nm per minutes, it is sufficient to remove the native oxide, which normally has the thickness of 2 to 3 nm.

Step 10 is polysilicon RIE. In this step, the polysilicon gates are patterned on the LAM490 etching system. The etching process has an etching rate of 20 nm per minute, an approximately 77 degree sidewall angle, and greater than 125 selectivity over the oxide (see section 4.3 for the details). The photoresist is stripped in acetone and IPA after the etching. The thickness of the polysilicon is so thin it is difficult to detect the polysilicon residuals by microscopic inspection. However, the polysilicon residuals will lead to shorts between the gates and the sources/drains, and cause the devices to fail. The field oxide is beneath the etched polysilicon, so once the polysilicon is cleared, the field oxide will be exposed. After the polysilicon etching, the etched regions are measured on

an optical thickness measurement system by using an oxide measurement recipe. If the GOF (goodness of fit) of the measurement is high, it indicates there are polysilicon residuals, and additional etching is needed. If the GOF is close to zero, it means that there are no polysilicon residuals, and the field oxide is fully exposed.

Step 11 is phosphorous doping. After the gate patterning, the polysilicon gates and the active regions are doped with phosphorous in a lateral diffusion furnace, and the gates act as the self-aligned mask to prevent the doping from going through the channel beneath. Two inch wafers are loaded and unloaded into a manual diffusion furnace at 1000°C without any temperature ramping cycle. Four inch wafers use an automatic diffusion furnace, and they are loaded and unloaded at 500°C with a temperature ramping cycle to 1000°C. The thickness of the polysilicon has been increased from 15 nm for two inch wafers to 40 nm for four inch wafers since the ramping cycle also consumes the polysilicon. The consumption of the polysilicon by the doping cycle was investigated (Table 4.1). There are three solid phosphorous doping wafers available in the furnace, and the silicon wafers are placed next to each doping wafer. Apparently longer diffusion time generates lower sheet resistance, and thicker phosphosilicate oxide. On average, 20 minutes diffusion can grow about 25 nm phosphosilicate oxide, and the phosphosilicate oxide thickness is measured by the ellipsometer thickness measurement system.

Step 12 is phosphosilicate glass removal. During the phosphorous doping, a layer of phosphosilicate glass is formed on the surface of the polysilicon. After the phosphorous doping, the wafer is dipped in 1:104 DHF at room temperature for 3 minutes to remove the phosphosilicate glass. The etching rate is greater than 20 nm per minute. Final field oxide thickness is measured after the phosphosilicate glass removal. After the filed oxide

is grown, the field oxide is thinned during the later steps like all the DHF etching steps, the poly gate etching step, the phosphorous doping step and the phosphosilicate glass removal step. Table 4.2 lists the field oxide thickness measured at each major step for the NMOS window isolation process.

Step 13 is SOG deposition. The SOG is used as the interlayer dielectrics. The ACCUGLASS SOG by Honeywell is applied to the wafer at 2000 RPM (rotation per minute) for 40 seconds, then the wafer is baked on the hotplate at 125°C for 3 minutes. Then the wafer is loaded into the Lindberg Blue burn-box at 250°C, and the temperature is ramped up to 400°C. At 400°C the wafer is hard-baked with nitrogen flow at 1 slpm for 60 minutes.

Table 4.1: Four inch wafers polysilicon doping experiment results

Split	Sheet Resistance Before Doping Sheet Resistance	Sheet Resistance After Doping	Phosphosilicate Oxide
10 minutes Wafer 1	34.4 Ohm/square	915.1 Ohm/square	11.0 nm
10 minutes Wafer 2	35.3 Ohm/square	724.8 Ohm/square	12.1 nm
10 minutes Wafer 3	34.0 Ohm/square	715.7 Ohm/square	12.5 nm
20 minutes Wafer 1	34.4 Ohm/square	271.8 Ohm/square	22.5 nm
20 minutes Wafer 2	38.1 Ohm/square	201.6 Ohm/square	25.0 nm
20 minutes Wafer 3	22.2 Ohm/square	194.8 Ohm/square	26.0 nm

Table 4.2: The field oxide thickness of the NMOS window isolation

Step	Wafer 1	Wafer 2	Wafer 3
After the field oxide growth	377.2 nm	374.5 nm	377.1 nm
After the gate polysilicon RIE	364.1 nm	354.9 nm	353.7 nm
After the phosphosilicate glass removal	278.9 nm	261.6 nm	271.2 nm

Step 14 is mask three lithography. The purpose of this step is to create contact holes from the metal contact pads to the substrate; the contact holes act as body contacts for the transistors. Since the dialectics (SOG + field oxide) thicknesses at the gates, and the active regions and the isolation regions are different, if all the contact holes in those areas are open at the same time, either the holes at the gates and the active regions are over-etched, or the holes at the isolation regions are under-etched. So it is necessary to open the contact holes at the different regions by using different masks. A positive photoresist is used at this step, and Appendix B details the process steps.

Step 15 is BOE etching. The wafer is bathed in 1:6 BOE at room temperature for 4.5 minutes. After the etching, an optical thickness measurement system is used to measure the oxide thickness at the open features to decide whether there are oxide residuals or not. The reading of the measurements should be close to zero. The photoresist is then stripped in acetone and IPA.

Step 16 is mask four lithography. The purpose of this step is to create the contact holes at the gates and the active regions. A positive photoresist is used in this step, and Appendix B details the process steps.

Step 17 is BOE etching. The wafer is bathed in 1:6 BOE at room temperature for 5.5 minutes. After the etching, an optical thickness measurement system is used to measure the oxide thickness at the open features to decide whether there are oxide residuals or not. The reading of the measurements should be close to zero. The photoresist is then stripped in acetone and IPA.

Step 18 is DHF etching. The wafer is dipped in 1:104 DHF at room temperature for 3 minutes to remove the native oxide before the aluminum sputtering. Before the metal is

deposited into the contact holes, it is necessary to ensure that the exposed silicon surface is as free as possible of contaminations and the native oxide. The native oxide can represent an impediment to the current that flows through the contact interface, resulting in high resistance for the ohmic contacts. The native oxide layer can grow thicker in 30 to 60 minutes if the silicon is exposed to the atmosphere at room temperature [36]. Consequently, the native oxide layers must be removed, and the metal must be deposited quickly enough after the pre-metal cleaning that the native oxide does not have enough time to regrow.

Step 19 is aluminum sputtering. A 500 nm aluminum (with 1 wt% silicon) is deposited by using the Denton Discovery 18 Sputtering System at 2×10^{-6} torr pressure, 100W RF power with argon flow for 20 minutes. The deposition rate is about 25 nm per minute. The thickness of the aluminum film is measured by the Tencor P-10 Profilometer.

Step 20 is mask five lithography. The purpose of this step is to define the aluminum interconnections between the gates, the sources, the drains and the substrate. A positive photoresist is used, and Appendix B details the process steps.

Step 21 is aluminum etching. The aluminum is etched in an etchant mixed with phosphoric acid, nitric acid, acetic acid, and DI water at a ratio of 16:1:1:2 at room temperature for 5 minutes. The photoresist is then stripped in acetone and IPA.

Step 22 is contact annealing. In this step, the contacts are annealed in the Lindberg lateral furnace at 400°C for 40 minutes with a forming gas (2% hydrogen, 98% argon). Besides, this annealing step with a forming gas can reduce the level of the interface trap density, D_{it} (see Appendix A).

Fig. 4.2 shows an image of a die on a completed device wafer.

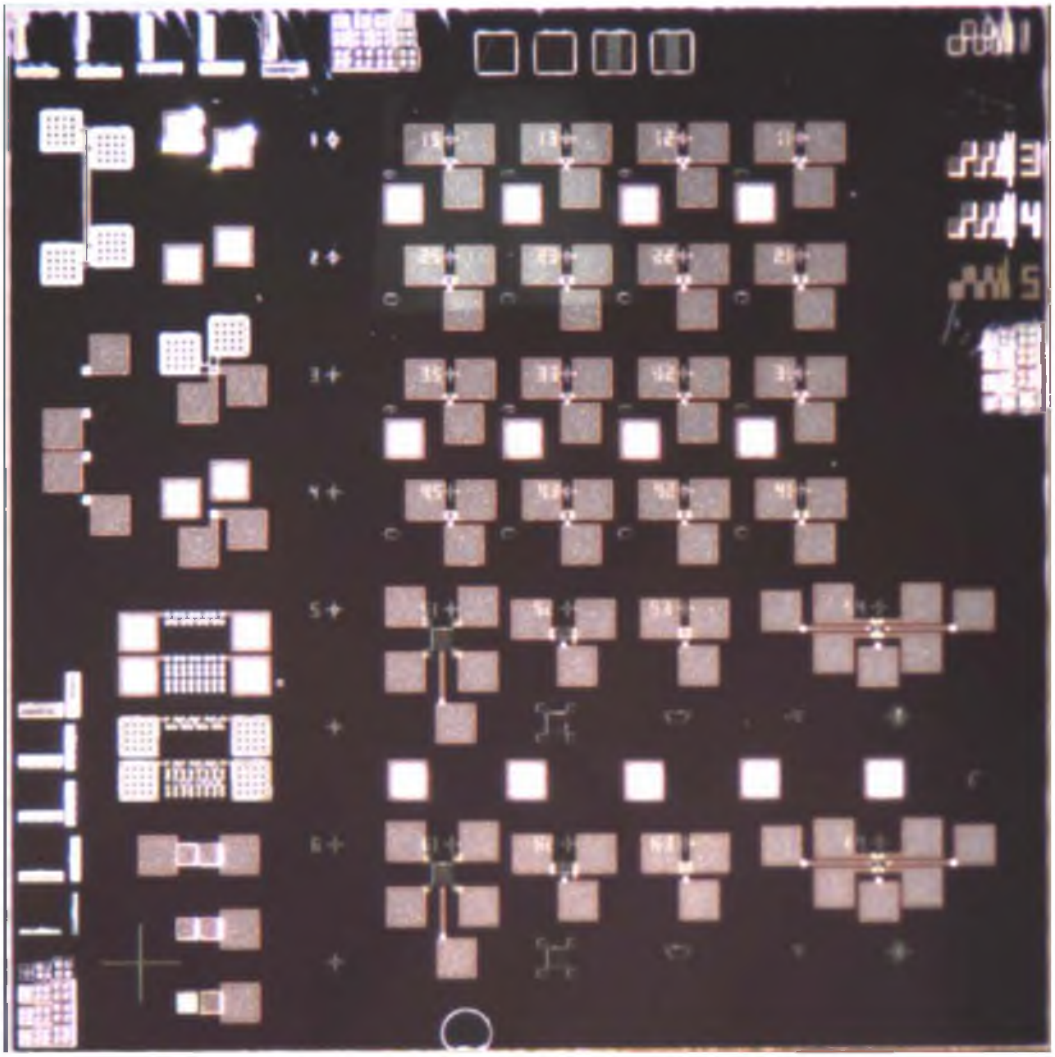

Fig. 4.2: Image of a die of an NMOS window isolation device wafer

4.2.2 NMOS Window Isolation Characterization

The NMOS window isolation transistors were fabricated by using both the two inch and the four inch NMOS processes. Fig. 4.3 shows the image of a fabricated NMOS transistor.

The V_{ds}-I_{ds} characteristics are shown in Fig. 4.4 and Fig. 4.5, and this lays the foundation for the future MOSFENS device fabrication.

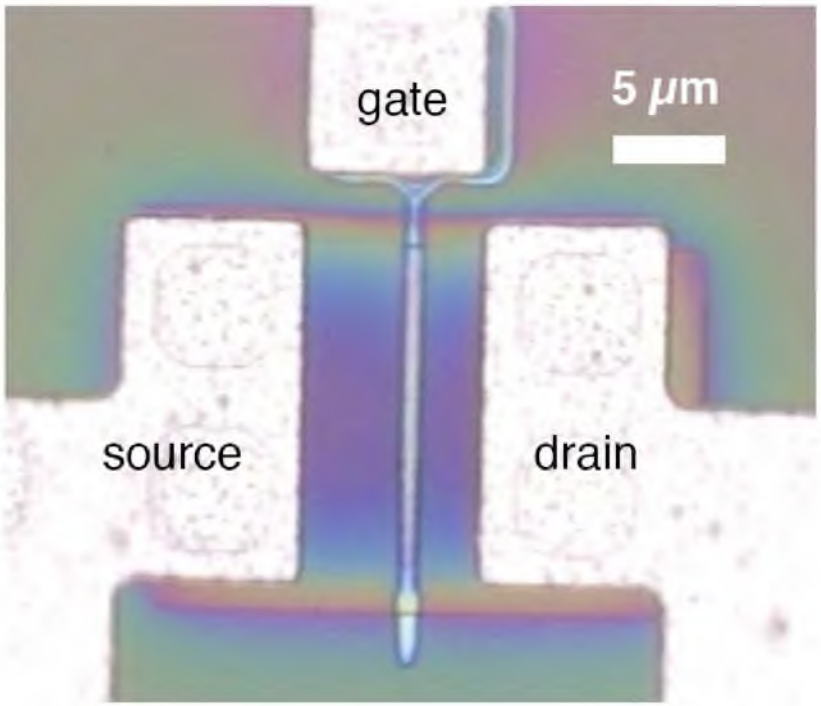

Fig. 4.3: Top view of a polysilicon gate NMOS window isolation transistor

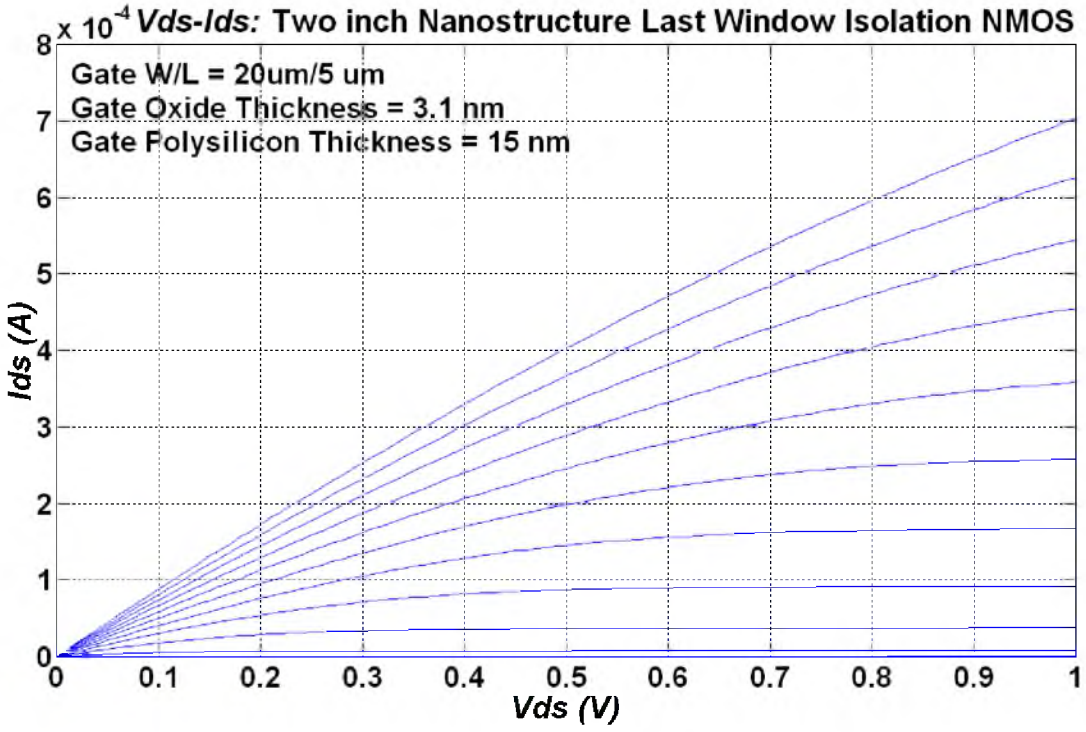

Fig. 4.4: Two inch nanostructure last window isolation NMOS V_{ds}- I_{ds}

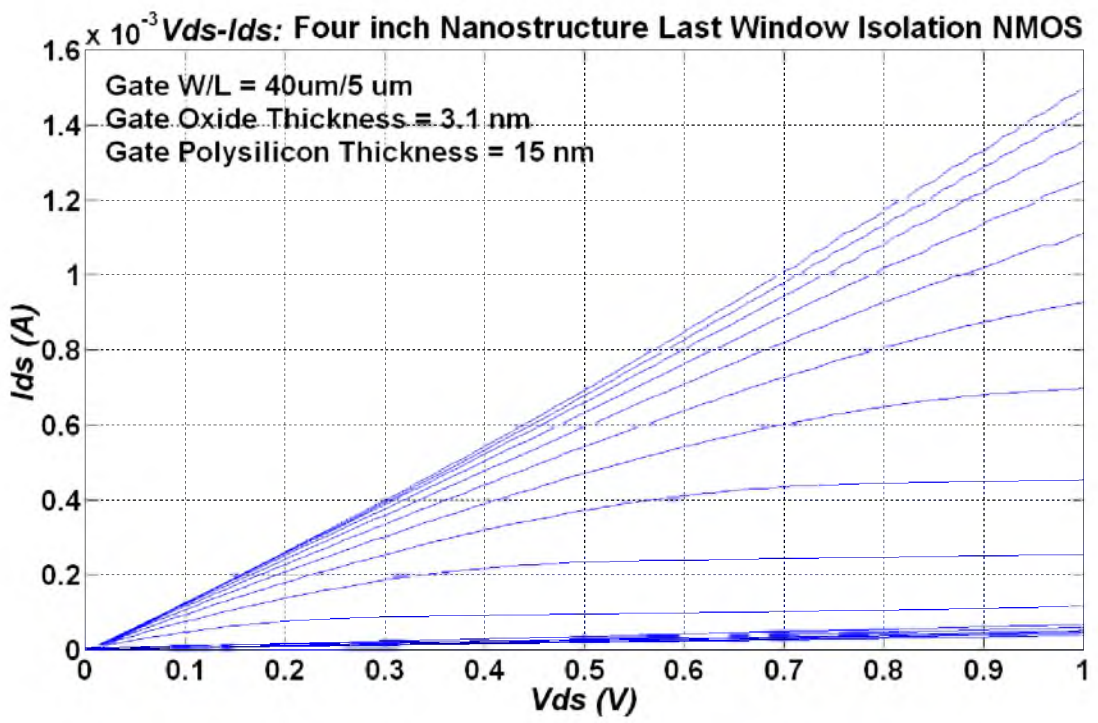

Fig. 4.5: Four inch nanostructure last window isolation NMOS V_{ds}- I_{ds}

4.3 NMOS Mesa Isolation Process Flow and Characterization

In this section, the process flow of the NMOS mesa isolation is presented, followed by the characterization results.

4.3.1 NMOS Mesa Isolation Process Flow

The process steps of the NMOS mesa isolation for the four inch wafers are described step-by-step below.

Step 1 is wafer start. Four inch *p* type CZ (Czochralski) silicon substrates with boron dopants and <100> crystal orientation are used. The resistivity of the substrates is between 1 to 5 Ω-cm.

Step 2 is DHF sip. The wafer is dipped in 1:104 DHF at room temperature for 2 minutes to remove the native oxide.

Step 3 is mask one lithography. The purpose of this step is to define the active regions and the nonactive regions (the trenches) as shown in Fig. 4.6. A positive photoresist is used, and Appendix B details the process steps.

Step 4 is silicon trench RIE. After mask one lithography the active regions are protected by the photoresist. The wafer is etched by the LAM490 system using SF_6 gas at an 80 sccm flow rate with inert helium gas at a 120 sccm flow rate. The chamber pressure is set at 2 torr and the RF (radio frequency) top power is set at 200W. The depth of the trenches is about 290 nm after 45 seconds of etching. Fig. 4.7 shows the cross-section view post silicon trench RIE. The photoresist is then stripped in acetone and IPA.

Step 5 is field oxide growth. A 370 nm field oxide is thermally grown in a lateral oxidation furnace by using the wet oxidation technique at 1000°C for 70 minutes to fill the trenches (Fig. 4.8).

Step 6 is CMP (chemical mechanical polishing): The CMP technique is used to flatten the trenches (Fig. 4.9). A silica-based oxide slurry, DCM-D37 with 1:1 dilution

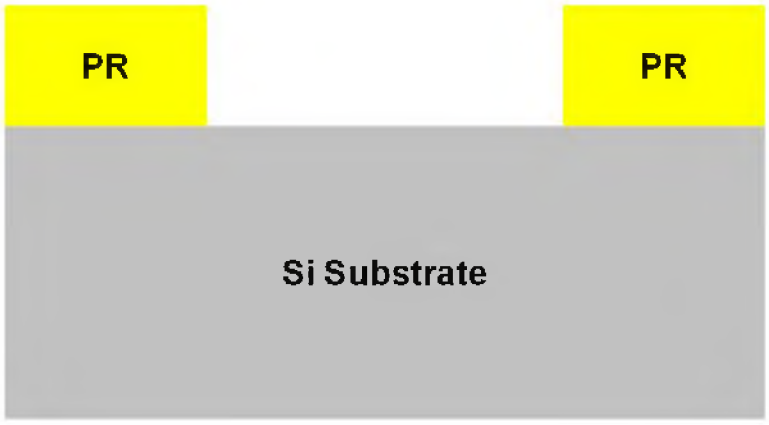

Fig. 4.6: NMOS mesa isolation: mask one lithography

Fig. 4.7: NMOS mesa isolation: silicon trench via RIE

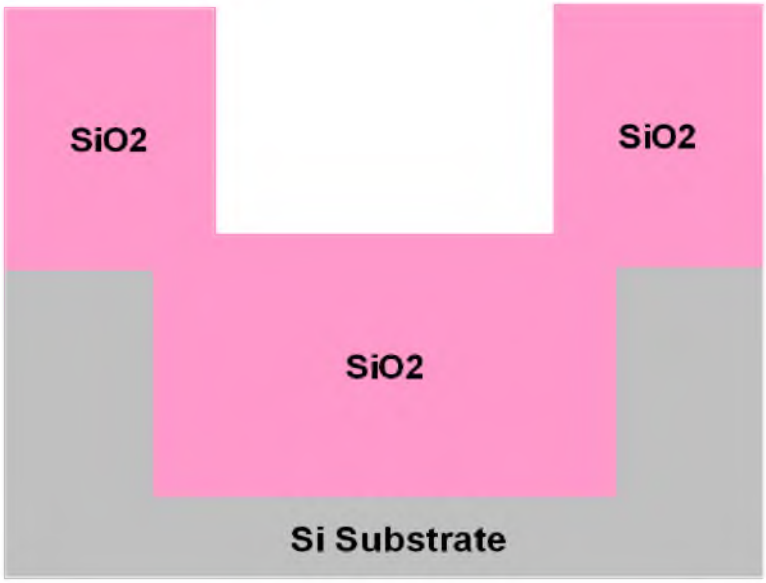

Fig. 4.8: NMOS mesa isolation: field oxide growth

Fig. 4.9: NMOS mesa isolation: CMP

with DI water on a dual stacked X-Y grid-grooves polishing pad is used. The process has a polishing rate of approximately 135 nm per minute on 1000°C grown wet oxide. The process uses 50 RPM on the chuck and the platen rotation, 5 psi downforce and the slurry flowrate is 175 ml per minute (see section 5.5).

An optical thickness measurement tool is used to measure the oxide remaining on the active regions after CMP. The purpose is to make sure the oxide on the active region particles, metal contaminants, all undesirable for the remaining steps; therefore, the wafer is subjected to the post-CMP cleaning steps to return the wafer surface to an acceptable cleanliness level. For the post-CMP cleaning, 1:104 DHF solution at room temperature is used to remove the slurry particles and the metallic contaminations.

Step 7 is sacrifice oxidation. A 30 nm wet oxide is grown to get rid of the CMP introduced defects. The wafer is loaded and unloaded at 500°C, and the oxidation is performed at 1000°C for 2 minutes.

Step 8 is DHF etching. The wafer is dipped in 1:104 DHF at room temperature for 12 minutes to remove the sacrifice oxide. The reason for using DHF not BOE, is to have a better control of over-etching. It is critical to completely remove the sacrifice oxide on the active regions before the gate oxidation, but it is also very important to reduce the amount of over-etching as much as possible to minimize the step height. As mentioned above, any residual oxide before the gate oxidation will be added to the 3 nm gate oxide, which will cause an increase in overall gate oxide thickness which would cause shifts between the predicted and the actual performance. Since it is impossible for microscopic inspection to detect the nanometer scales oxide residuals, an optical thickness measurement is applied to make sure the oxide thickness readings on the future gate

regions are zero.

From the next step (the gate oxidation) on, all the steps are exactly the same as the ones of the NMOS window isolation process of section 4.2.

Table 4.3 and 4.4 show the field oxide thickness measured at each step and the final step height before the EBL. As shown above, the CMP introduced step height is actually much smaller compared to the step height generated by the sacrifice oxide removal and the gate polysilicon RIE. The reason is that both steps use sufficient over-etching to make sure the oxide and the polysilicon are cleared.

Table 4.3: Trench oxide thickness of the NMOS mesa isolation

Step	Wafer 1	Wafer 2	Wafer 3
After Trench Oxide Growth	378.3 nm	387.8 nm	397.0 nm
After CMP	293.9 nm	307.0 nm	311.6 nm
After Gate Polysilicon RIE	223.0 nm	243.9 nm	219.2 nm
After Phosphosilicate Glass Removal	181.6 nm	200.7 nm	175.6 nm

Table 4.4: Step height of the NMOS mesa isolation

Step	Wafer 1	Wafer 2	Wafer 3
After STI Trench RIE (= Trench Depth)	-327.3 nm	-323.2 nm	-327.6 nm
After CMP	-33.4 nm	-16.2 nm	-16.0 nm
After Sacrifice Oxide Removal	-120.5 nm	-74.4 nm	-78.4 nm
After Gate Polysilicon RIE	-163.7 nm	-159.6 nm	-129.4 nm
After Phosphosilicate Glass Removal	-173.1 nm	-174.5 nm	-192.2 nm

4.3.2 NMOS Mesa Isolation Characterization

The NMOS mesa isolation transistors were also fabricated, but all the transistors failed. The measurement results are plotted in Fig. 4.10.

The V_{ds} vs. I_{ds} characteristics of the mesa isolation transistors show that the channel current does not change when the gate voltage varies, and there is no isolation between the gates and the drains/sources. However, the window isolation transistors show good

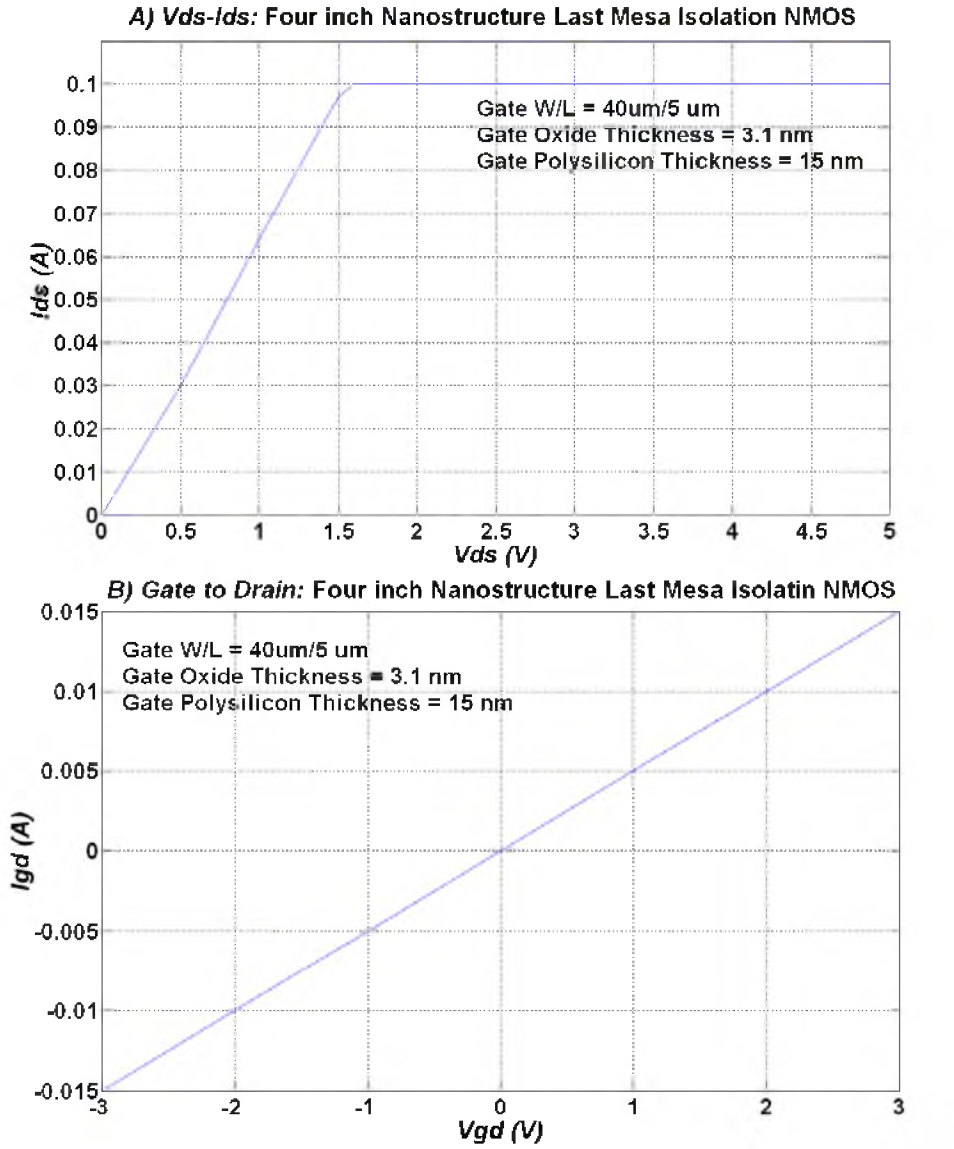

Fig. 4.10: Four inch NMOS mesa isolation characteristics

isolation between the gates and the drains/sources, and these transistors are working fine. Since the window isolation transistors and the mesa isolation transistors grow the gate oxide and the gate polysilicon in the same batch, this indicates that the gate oxide and the gate polysilicon have no problems. Hence, for the mesa isolation, we conclude that the gate polysilicon is shorted with the substrate caused by the following mechanisms. Firstly, the sharp corners at the top of the trenches generate a higher electrical field [37], and it tends to grow thinner oxide [38], which is susceptible to break-down and consequently leads to a short between the gate polysilicon and the substrate (Fig. 4.11). Secondly, the substrate of the upper portion of the trenches was exposed during the trench RIE etching, and it was subjected to plasma damage. Thus, the gate oxide grown there could contain more traps and defects, and consequently lead to oxide break-down and a short between the gate polysilicon and the substrate (Fig. 4.11).

To solve this issue, a trench filling technique with HDP (high density plasma) oxide [39] needs to be used. The comparison between a standard STI process using HDP filling and the mesa isolation process are schematically illustrated in Fig. 4.12 and Fig. 4.13.

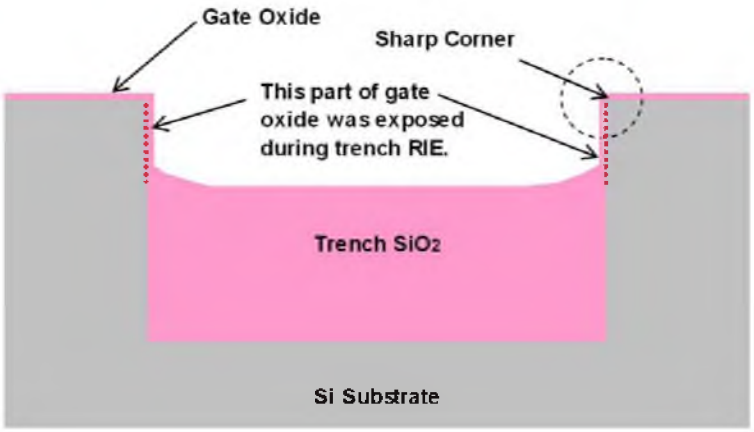

Fig. 4.11: Reasons for the mesa isolation transistors failure

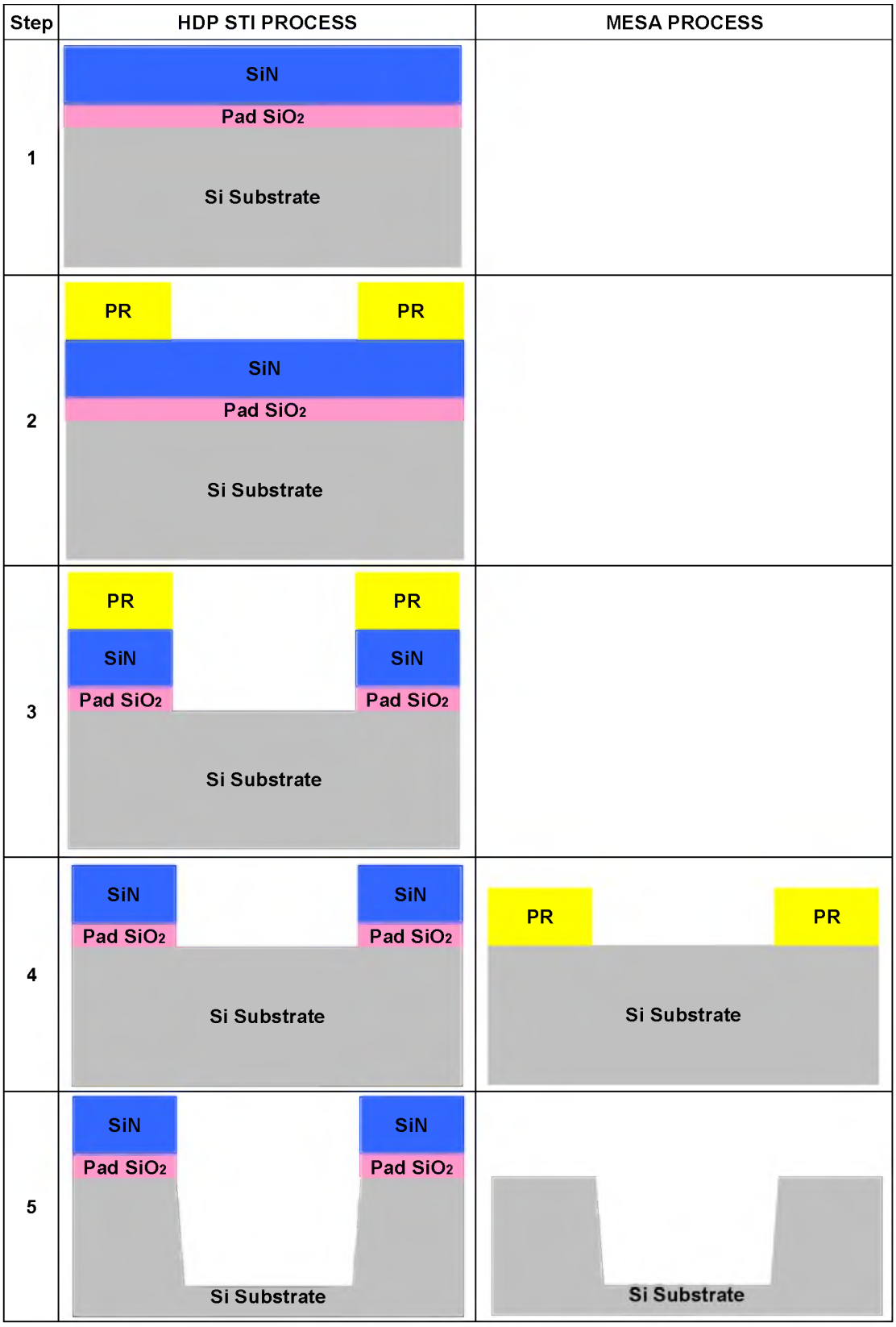

Fig. 4.12: Comparison between the mesa process and a STI process, steps 1 to 5

Fig. 4.13: Comparison between the mesa process and a STI process, steps 6 to 10

4.4 Thin Polysilicon Gate and Nano-LOCOS Compatibility Experiment

As mentioned above, both the nanostructure last and the nanostructure first have an undulating Si-SiO_2 interface to confine the electrons to the sites, which will be created by the nano-LOCOS process. An experiment was carried out to examine the compatibility between the thin gate polysilicon and the nano-LOCOS process.

Table 4.5 shows the information of the experimental splits. Wafer C was processed with all the steps, and wafer A did not have the in-situ POA after the nano-LOCOS. Wafer B did not have nano-LOCOS and the following in-situ POA, and wafer D only has the gate oxide and the unthinned polysilicon gate electrode.

The transistors of wafer D failed due to contact failure. As shown in Fig. 4.14, the transistors of wafer A, B and D are functioning but have significant differences in the sub-threshold current. Single oxidation and annealing split, wafer B has the biggest subthreshold channel current, while double oxidation and single annealing split, wafer A has a slightly reduced sub-threshold current. The split of double oxidation and double annealing split, wafer C has the smallest sub-threshold current in the range of 1 μA.

Table 4.5: Thin polysilicon gate and the nano-LOCOS compatibility experiment splits

Step	Wafer	A	B	C	D
1	3 nm gate oxide growth	√	√	√	√
2	In-situ POA	√	√	√	√
3	40 nm gate polysilicon growth	√	√	√	√
4	25 nm polysilicon thinning	√	√	√	×
5	Nano-LOCOS	√	×	√	×
6	In-situ POA	×	×	√	×

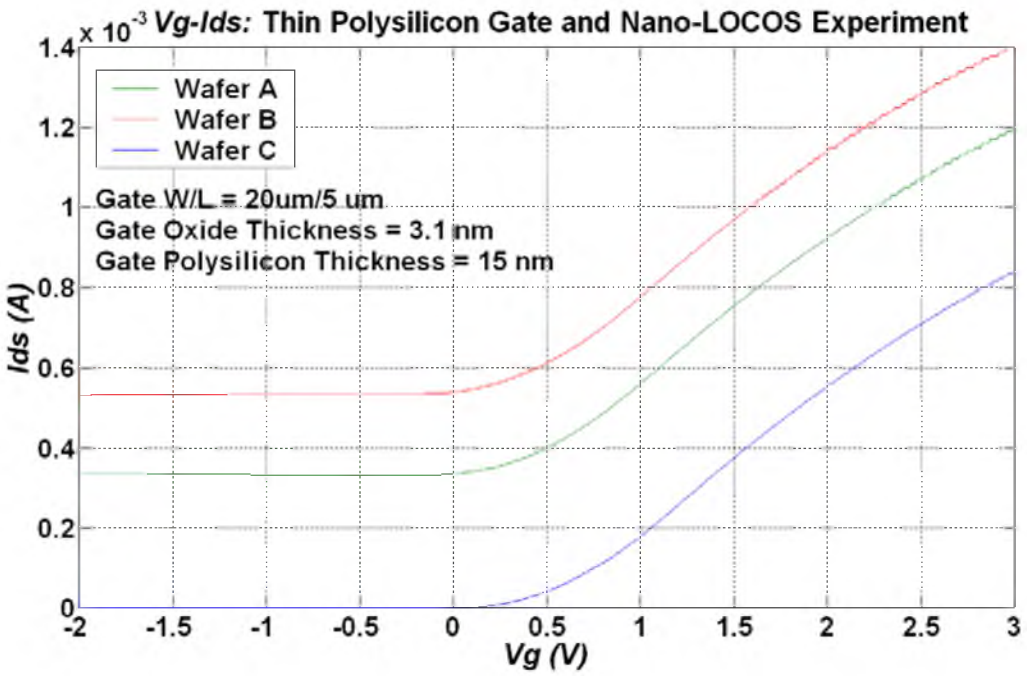

Fig. 4.14: Thin polysilicon gate and the nano-LOCOS compatibility experiment: V_g-I_{ds}

The results can be interpreted as following mechanisms. Firstly, annealing is more effective compared to oxidation in eliminating interface charges and traps, and the second annealing is needed to reduce the sub-threshold current to an acceptable level. Therefore, it was decided to use POA for both the gate oxidation and the nano-LOCOS. Secondly, the 3nm gate oxide is at the border of the reliable operating regime, and small variations from the processing (like wafer cleaning) could lead to big differences in the sub-threshold current.

4.5 Conclusions

The window isolation process makes working transistors, and it sets the cornerstone for MOSFENS devices fabrication. The transistors fabricated by using the mesa isolation characteristics failed, and it is concluded that the failures were caused by the short

between the gate polysilicon and the substrate. This issue will be solved by a CVD (chemical vapor deposition) type trench-fill technique. Additionally, the results of the experiment show that the thin gate polysilicon film is compatible with the nano-LOCOS process, which was invented for this work to provide a practical route to engineer and manipulate the in-plane electrons profile.

CHAPTER 5

NANOSTRUCTURE PROCESS DEVELOPMENT

MOSFENS spin lattices process integration challenges come from the practical difficulties in modifying an established NMOS fabrication process (see Chapter 4), to accommodate the interface patterning requirements. This chapter introduces the development of those modifications including the thin oxidation for both gate oxide growth and the nano-LOCOS process, thin polysilicon deposition and etching, EBL used to pattern the spin lattices on the gates and CMP process used in the mesa isolation to planarize the oxide in the trenches.

5.1 Thin Oxidation for Gate Oxide and Nano-LOCOS

As stated above, the nano-LOCOS was invented to give a practical route to engineer and manipulate the electron profile at the Si-SiO_2 interface, and it uses a thin oxidation process to create nanometer scale isolation between the sites. After the polysilicon spin lattice etching, the wafer is put into a lateral oxidation furnace at 800°C for 8 minutes using the dry oxidation technique. After the oxidation, the furnace is ramped up to 1050°C, and kept at 1050°C for 10 minutes to anneal the traps and the fixed charges at the Si-SiO_2 interface. As result, a 3 nm oxide will only grow on the open silicon substrate

(Fig. 5.1). This process is very similar to the standard LOCOS process, but it is implemented on a much smaller scale. The same process is used for the thin gate oxide growth.

A thin oxidation process has been characterized and studied. The results are compared to the prediction using Reisman-Nicollian power-law Model [40] (Fig. 5.2). The difference in thickness could be caused by many factors, like the accuracy of temperature control, time lag in turning on and turning off the oxygen [41].

The oxide thickness is measured by the VASE (variable angle spectroscopic ellipsometer) made by Woollam Spectroscopic. This instrument has small spot focusing optics and an automated X-Y translation stage. The ellipsometry technique makes use of the change of state of the polarization of light when it is reflected from the film surface. The state of polarization is determined by the relative amplitude of the parallel and perpendicular components of the radiation, and by the phase difference between these

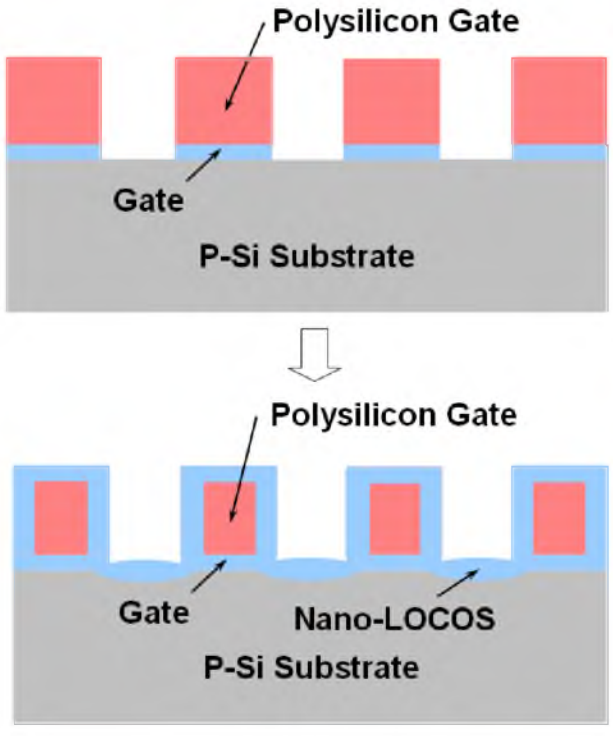

Fig. 5.1: Creating nanoscale isolation by using the nano- LOCOS process

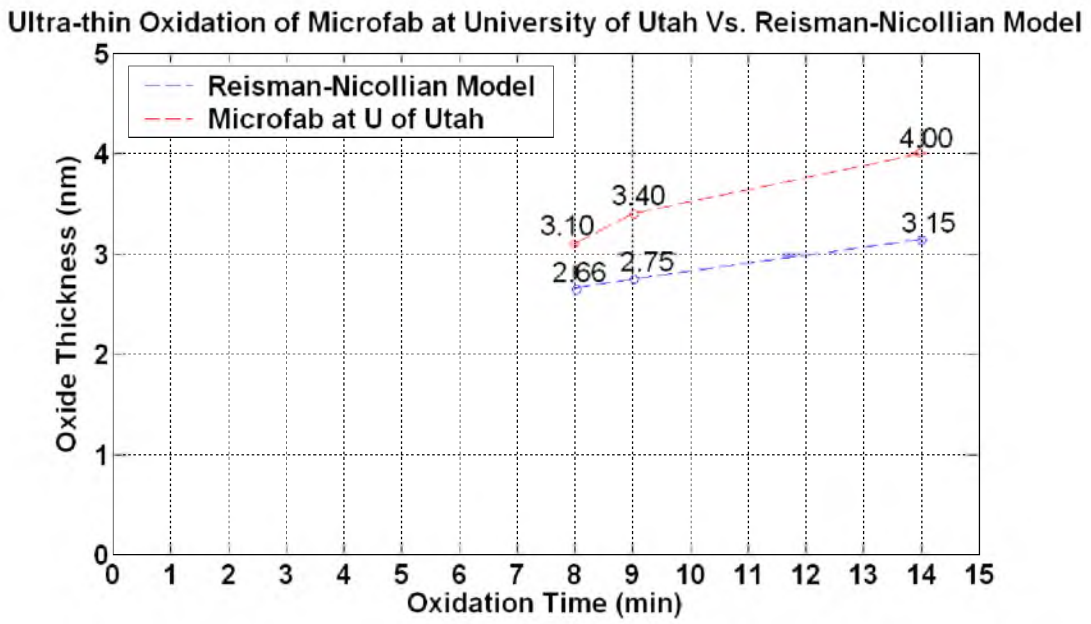

Fig. 5.2: Thin oxidation thickness versus Reisman-Nicollian model

two components. The polarization change depends on the optical constants of the silicon,the angle of incidence of the light, the optical constants of the film, and the film thickness [42].

5.2 Thin Polysilicon Deposition

The reason of setting the thickness of the polysilicon to 15 nm is to obtain a reasonable aspect ratio during the polysilicon spin lattices etching. Before the thin polysilicon deposition process was developed, a 50 nm polysilicon film was deposited first, then wet etching was used to thin the thickness of the polysilicon to 15 nm. The etchant is mixed by HNO_3, H_2O and NH_4F with the ratio of 126:60:1, and the etch rate is 30 to 40 nm per minute. However, the wet etching process is extremely unstable because of the following reasons. Firstly, it is difficult to precisely control the concentration of NH_4F, which has a drastic impact on the etching rate. As an example, etching in the

etchant with two parts NH_4F instead of one part NH_4F, the etching rate of the polysilicon increases dramatically from 30 to 40 nm per minutes to > 220 nm per minute. Secondly, the etching uniformity across the wafer is poor. The chemical reaction generates a lot of heat, and needs to agitate the etchant constantly to disperse the heat. A region with high temperature without appropriate agitation generates a higher etching rate, and leads to nonuniformity within the wafer. Additionally, the etchant needs to be cooled down hours after it has been mixed. Furthermore, the temperature of the etchant keeps increasing during the etching. In order to obtain a constant etching rate, it needs to wait for the etchant to cool down before etching the next wafer. Finally, the etchant has a short shelf life, and the etching rate deteriorates quickly after a couple of runs. Hence, the etchant needs to be replenished constantly.

Consequently, it is necessary to examine the possibility of depositing a 15 nm thin polysilicon film directly. A thin polysilicon deposition process was developed with a slow deposition rate of around 4 nm per minute with a lateral LPCVD (low pressure chemical vapor deposition) furnace. The deposition temperature is 630°C, and the deposition base pressure is set at 80.4 mV. The pressure controller set point is 150 V with a silane flow rate of 20 sccm. The higher the silane flow rate is, the higher the deposition rate is. However, it was revealed that 15 nm polysilicon would be totally consumed during the following doping cycle, so the thickness of polysilicon film was changed to 40 nm to accommodate this finding.

5.3 Thin Polysilicon RIE

A key process to develop and integrate is the controlled dry etching of the spin lattice pattern through the thin polysilicon gates. The polysilicon gates are patterned by using

the RIE process on a LAM490 etching system. A practical and effective polysilicon etching process on a gate stack of a 3 nm gate oxide and a 15 nm polysilicon should have the following characteristics.

Firstly, polysilicon etching rate is approximately 20 nm per minute. This allows long enough etching time (> 30 seconds) to have a wider process control window.

Secondly, the process should have a high selectivity between the polysilicon and the gate oxide, ideally > 50. As an example, for 20 nm per minute polysilicon etching rate with a selectivity to the oxide at 50, the oxide etching rate is 0.4 nm per minute. Thus, a 3 nm thick oxide should be able to stand 7 minutes of over-etching. High selectivity over the oxide will prevent the gate oxide undercut from happening during the etching, which directly causes the shrink of the gate width and a possible short between the polysilicon gates and the channels. Also, it protects the silicon substrate during the entire etching process and avoids plasma etching damages, which could consequently cause the failure of the following nano-LOCOS oxide.

Finally, the process should have an anisotropic sidewall profile. For the spin lattices, it is paramount to faithfully reproduce the dimension of EBL features to the holes on the polysilicon. A polysilicon etching process must exhibit excellent line and width control, in other words, have anisotropic sidewall profiles. The anisotropic etching profile is not critical for the gate patterning based on the fact that the features are much larger in dimension (in microns) than the thickness of the film (in nanometers). The etching process has been optimized for the best anisotropic profile that can be obtained, in a sense, that same process will be used for both the polysilicon gate patterning and the polysilicon spin lattices etching.

It is known as loading effect that the plasma etching rate is directly proportional to the area of exposed etch surface, and the etching rate decreases as more etched surface is added [43]. Thus, it is expected that the etching rate will increase on much smaller spin lattices holes.

Process characterization is carried out for the polysilicon RIE process. This process uses chlorine gas on the LAM 490 AutoEtch etching system. Parameters like gas flowrate, mix ratio between chlorine and helium (inert gas), gap distance, and RF top power have been varied to understand their influences on the etching rate and the sidewall profile. As a summary, at 300 W, severe undercuts are observed, and at 200 W, no undercuts are found. It was also found that low gap distance generates undercut too. Besides, the higher the chlorine ratio in the mixture of chlorine and helium is, the lower the etching rate is and the straighter the sidewall profile is.

An optimized etching process with the best sidewall profile has been acquired. It has a 20 nm per minute etching rate, approximately 77 degree sidewall angle (Fig. 5.3), and the selectivity to oxide greater than 125. The details of the recipe are listed in Table 5.1, and a step-by-step description is presented below.

Step 1 is to pump the chamber down to 60 mTorr and to vent the oxygen remaining in the chamber. Step 2 is to turn on the RF power, and meanwhile to turn on the gas flow. Step 3 is the main step of the etching. In step 4, chlorine is turned off, and C_2F_6 is turned on. The C_2F_6 serves as a source of "recombinant," and it suppresses lateral etching by recombining with chlorine atoms, which have been adsorbed on the etched polysilicon sidewalls. Etching can proceed in the vertical direction because the ion bombardment from the plasma suppresses the recombination mechanism [44]. In step

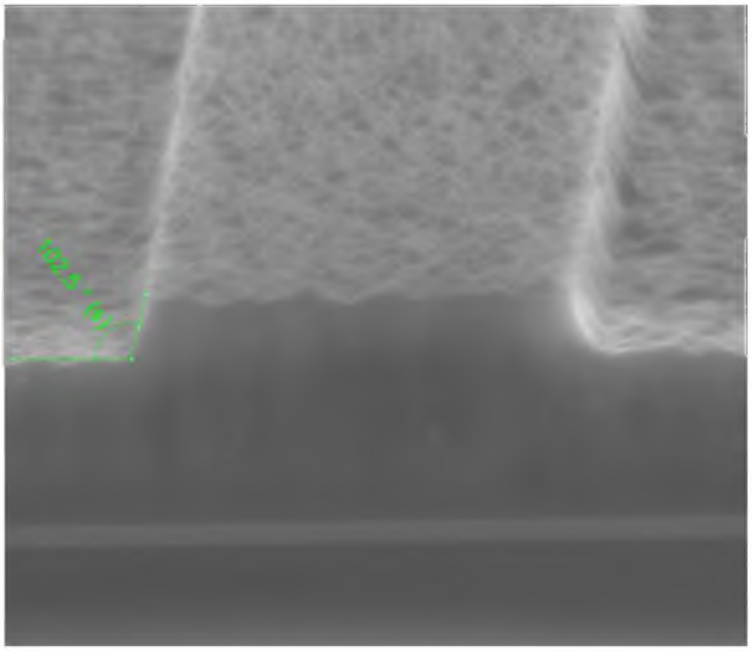

Fig. 5.3: Anisotropic profile via the polysilicon RIE

5, C_2F_6 is turned off, and helium flow rate is increased to 200 sccm to purge out the etching gases. From step 2 to step 5, the total gases flow stays at 200 sccm while the ratio of the gas mixture keeps changing. In this way, the pumping speed of the chamber stays steady, and there will be no turbulence inside the chamber that could cause instability in etching performance. In step 6, helium is turned off, and the chamber is pumped down to 20 mTorr before unloading the wafer.

Table 5.1: The polysilicon RIE recipe

Step	Pressure (T)	RF Top (W)	Gap (cm)	Cl_2 (sccm)	He (sccm)	C_2F_6 (sccm)	Time (m:s)
1	0.06	0	1.5	0	0	0	0:20
2	2	200	1.5	80	120	0	0:10
3	2	200	1.5	80	120	0	Time
4	2	225	1.5	0	100	100	0:05
5	1	0	1.35	0	200	0	0:30
6	0.01	0	1.35	0	0	0	1:00

5.4 Electron Beam Lithography

Electron beams can be focused to a very small diameter, and such finely focused electron beams can be readily scanned and accurately positioned on a wafer to expose a radiation-sensitive electron beam resist. To write small features, the electron beam must be generated, and focused into a small diameter spot. To obtain short resist exposure time, the current density in the focused spot must also be high. The electron beam is produced by an electron source (or an electron gun). There are also various lenses used to focus and magnify or demagnify the beam, and various apertures to limit and shape the beam, and a beam deflection system to position the beam on the wafer. In order to write over the entire wafer, a mechanical stage is used to position the wafer under the electron beam. The position of the stage must be accurately known at all times, and this position is usually controlled by a laser interferometer.

The EBL system at The University of Utah is FEI Nova NanoSEM 630, which is capable of extremely small feature patterning. Fig 5.4 shows the holes with the size as small as 10 nm, while Fig 5.5 shows an array of 15 nm holes with 100 nm in period. At the lower left corner of each die there is a fiducial cross serving as the primary alignment mark for EBL. There are also small crosses located to the left of each row of the transistors and the testing structures. The EBL alignment mark for each individual device is illustrated in Fig. 5.6. The first digit of the label indicates which row the device locates, while the second digit of the label indicates the transistor gate width in microns. As an example, "45" indicates this transistor locates in the fourth row, and has a gate width of 5 μm. Find a cross located to the right of the label, and from the center of this cross go down 100 μm, this will be the right upper corner of the gate area.

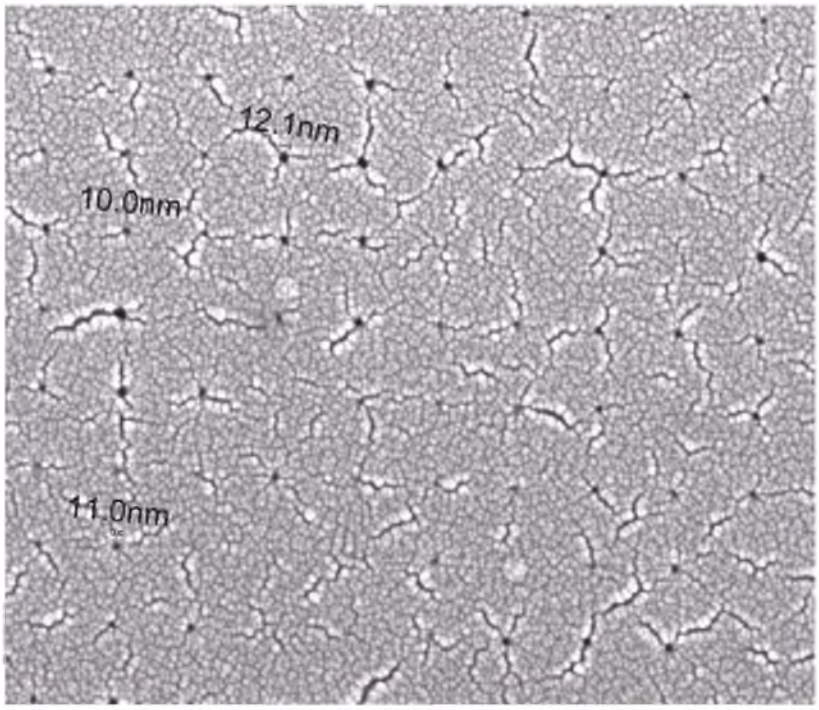

Fig. 5.4: Successful imaging of 10 nm holes by FEI Nova NanoSEM 630 (Courtesy of R. Polson, the Physics Department, The University of Utah)

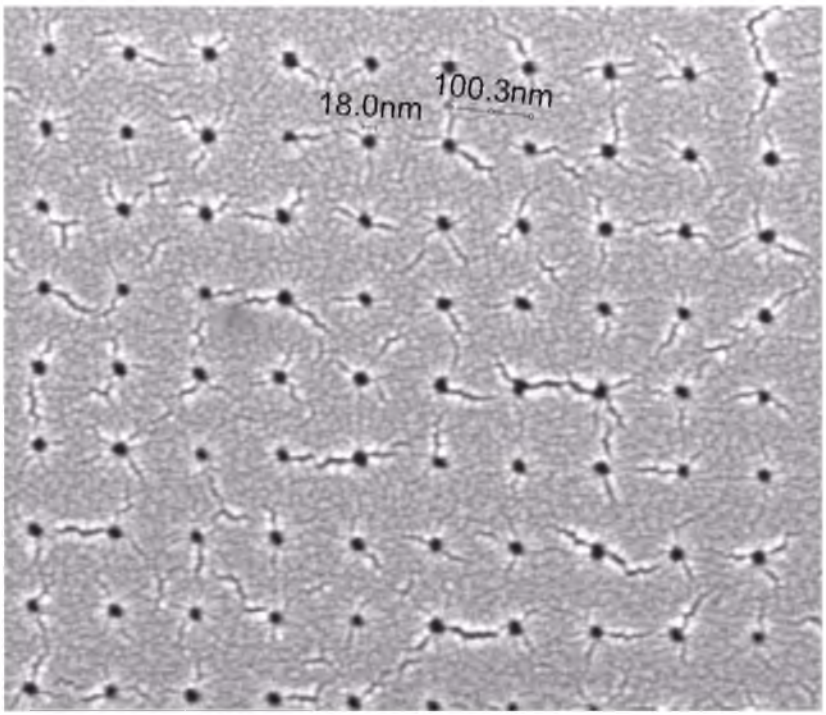

Fig. 5.5: Successful imaging of 15 nm holes with 100 nm spacing by FEI Nova NanoSEM 630 (Courtesy of R. Polson, the Physics Department, The University of Utah)

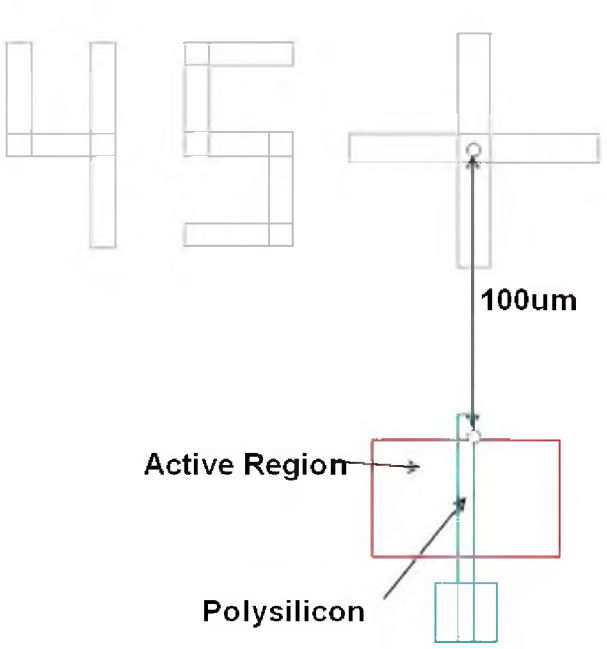

Fig. 5.6: EBL alignment mark for individual device

5.5 Chemical Mechanical Polishing

CMP plays a crucial role in planarizing the trenches for the nanostructure last mesa isolation. CMP is a process that provides local and global planarization with high elevation features being selectively removed resulting in topography with improved planarity. The tool used in the Nanofab of The University of Utah is Strasbaugh 6EC, which is a single head, single platen polisher. The structure of a typical CMP tool is schematically shown in Fig. 5.7.

A CMP process has been developed with good uniformity (approximately 6%, one sigma) and a reasonable polishing rate (approximately 135 nm per minute) on blanket oxide wafers. The process uses 50 RPM on chuck and platen rotation, 5 psi for the downforce and the slurry flow-rate is at 175 ml per minute. The polishing pad has X-Y grid grooves and a dual stacked IC-1000 hard pad and Suba-400 soft pad. A silica-based oxide slurry, Fujimi DCM-D37 with 1:1 dilution with DI water is used. However, due to

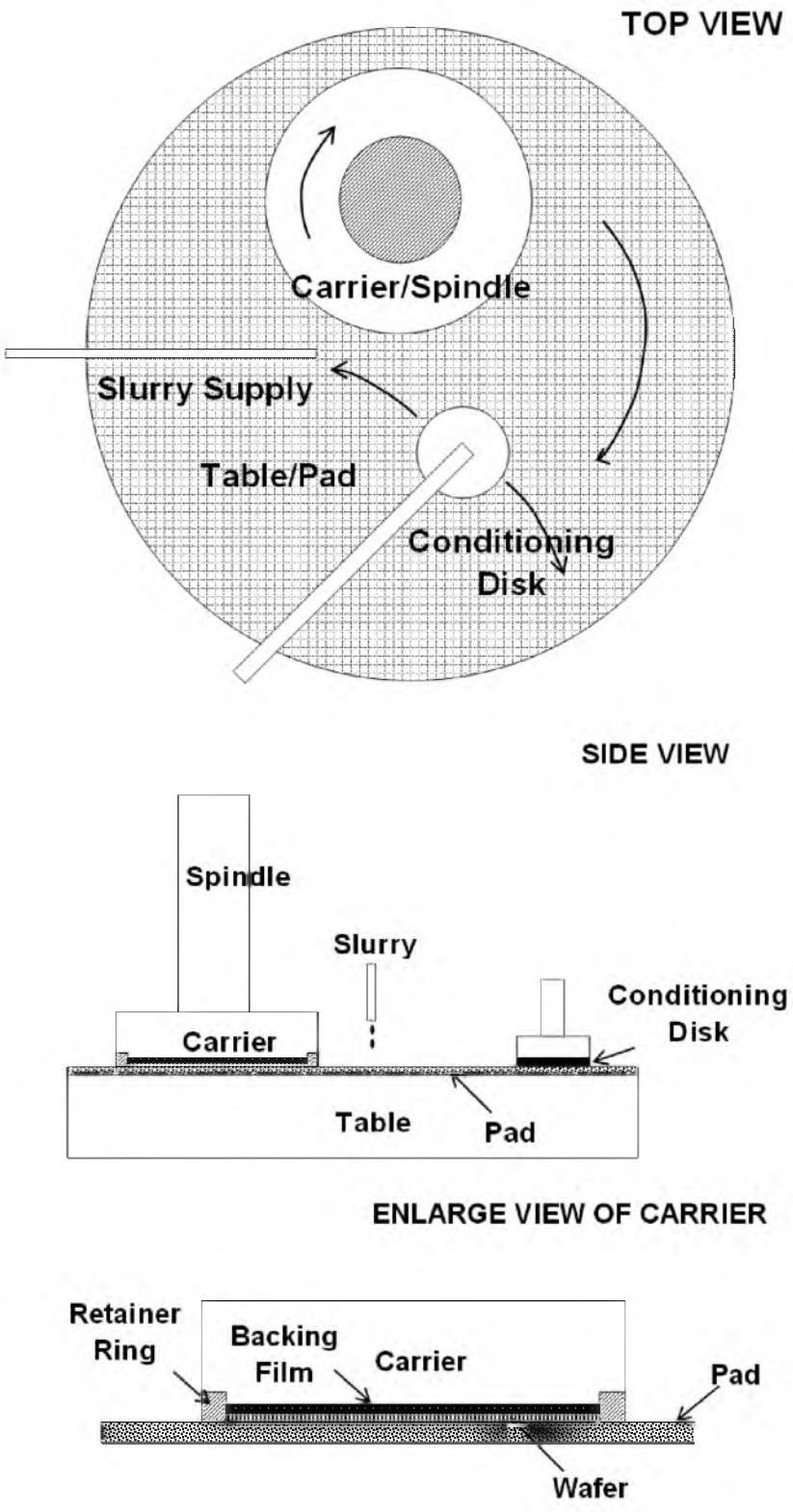

Fig. 5.7: Top view and side view of a CMP tool and enlarged view of the carrier

the protrusive active regions only making up to 20% of the total area of a wafer, a much faster polishing rate is observed for the active regions (about 330 nm per minute). This selective removal of materials that protrude above the surrounding topography is thought to arise from the compliant nature of the polishing pads. The polishing pad applies pressure to the wafer surface through the slurry, with the largest pressures being exerted where the pad is the most compressed. Higher pressure is applied to the elevated regions and the leading edges of the features, than to the lower-lying regions and the trailing edges. The difference in locally applied pressure causes differences in material removal rates. The smaller features are rounded off and polished faster than the wider features [45, 46].

5.6 Summary And Conclusions

Thin oxidation is used to grow the gate oxide and the nano-LOCOS, while the direct thin polysilicon deposition is able to avoid the difficulties of wet etching. Successful EBL on the optimal dimensions and the anisotropic polysilicon RIE ensure the spin lattice holes and arrays meet the design requirements. With all these processes characterized and developed, it is possible to fabricate MOSFENS devices by patterning the spin lattices on the polysilicon gates of the NMOS transistors, which were discussed in Chapter 4.

CHAPTER 6

NANOSTRUCTURE FABRICATION AND CHARACTERIZATION

Upon combining the NMOS process (Chapter 4) and the nanostructure processes (Chapter 5), MOSEFENS spin lattice devices were successfully fabricated. In this chapter, the fabrication process of MOSFENS spin lattice devices are introduced (section 6.1), and the characterization results are presented (section 6.2) with the calculations of the gate voltage Vg corresponding to different electron-per-site filling factor v. The MOSFENS spin lattice devices fabricated and presented here, use the nanostructure last design and window isolation. The lattices formation steps of the nanostructure first for future generations are introduced in Appendix C.

6.1 Nanostructure Last Fabrication Process

The lattice formation steps are described below.

Step 1 is electron beam lithography (EBL). A 100 nm PMMA (poly methyl methacrylate) resist (996000 molecular weight) by Aldrich Chemical is coated on the wafer, and it is pre-baked at 100 °C for 30 minutes before EBL. The patterning is done on the FEI Nova NanoSEM 630 with patterning controlled by a third party software package, NPGS (nanopattern generation system) by Nabity. The electron beam conditions are 30 kV with the current at 20 pA. A point dose of 2 fC is used to expose the resist.

Development of the resist is a 70 second bath in a 1:3 solution of 4-methyl-2-pentanone and IPA followed by a 20 second bath in IPA. Fig. 6.1 shows the cross-section view after the EBL.

Step 2 is spin lattices RIE. Before the etching, the wafer is baked at 105°C for 70 minutes to solidify PMMA resist to be able to stand the ion bombardment during RIE. The wafer is dipped in 1:104 DHF prior to the etching to remove the native oxide. The etching time is adjusted based on the pre-measured polysilicon thickness of each individual wafer. The wafer is bathed in acetone then IPA to remove PMMA resist, then the wafer is inspected to make sure there is no resist residual. Fig. 6.2 shows the cross-section view after the RIE.

Fig. 6.3 and Fig. 6.4 show the images before and after the spin lattices RIE of a MOSFENS device, which was fabricated using the nanostructure last and the window isolation process. This device consists of an array of 20 nm holes with 50 nm in period on the polysilicon gates patterned by EBL, then RIE.

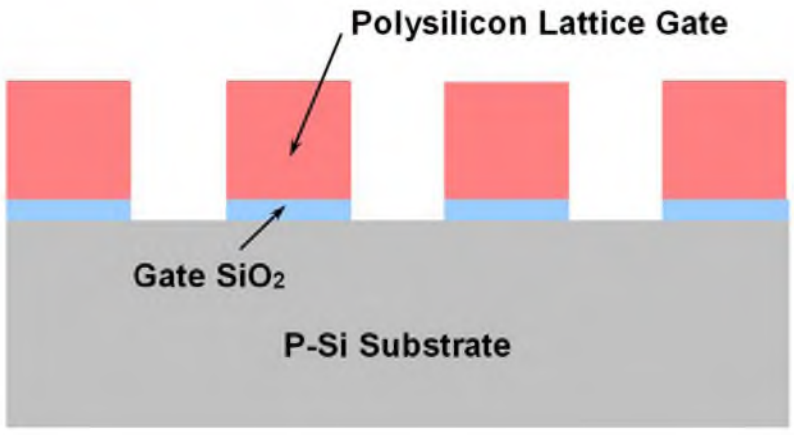

Fig. 6.1: The nanostructure last lattice formation: EBL

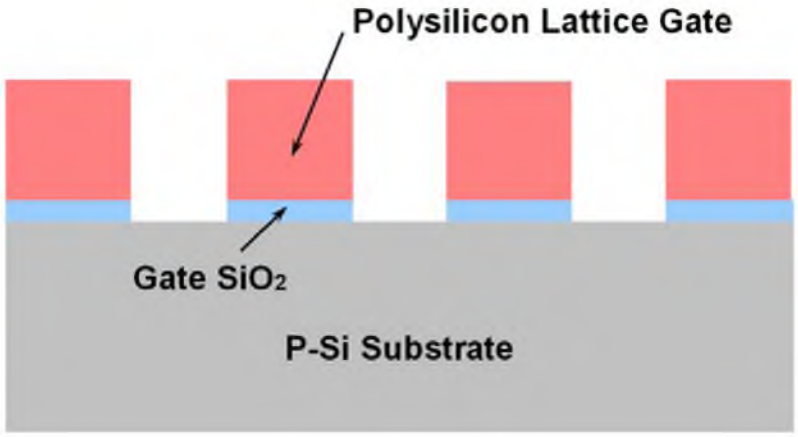

Fig. 6.2: The nanostructure last lattice formation: the spin lattices polysilicon via RIE

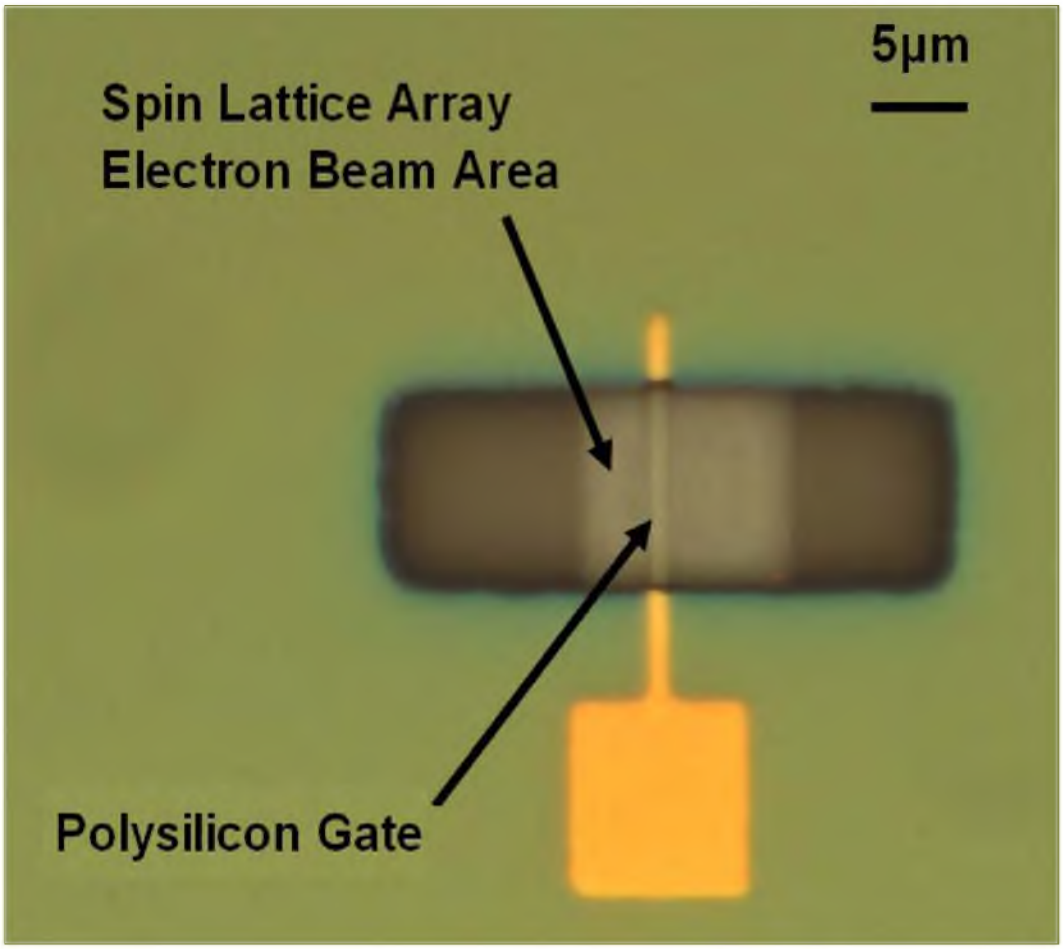

Fig. 6.3: Patterning on the polysilicon gate by EBL before the spin lattices undergo RIE

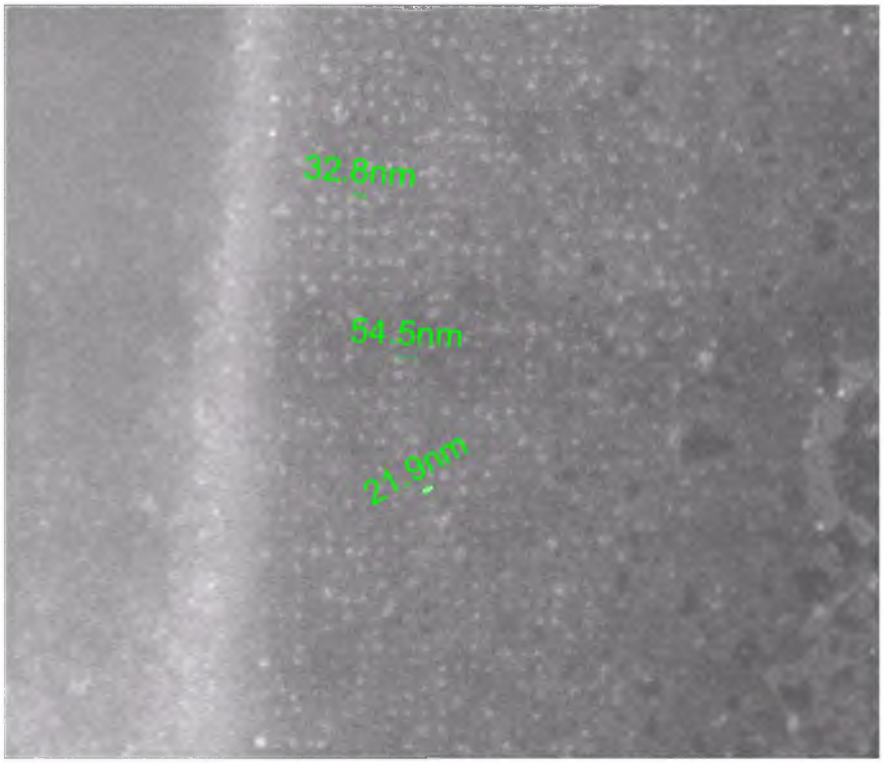

Fig. 6.4: Spin lattices holes (20 nm in size with 50 nm in period) on the polysilicon gate after the spin lattices RIE and PMMA resist strip (Cooperated with R. Polson, the Physics Department, The University of Utah)

Step 3 is nano-LOCOS. The nano-LOCOS is developed to create an undulating Si-SiO_2 interface to confine the electrons, and it uses thin oxidation to form nanometers scale isolation between the lattices (Fig. 6.5). As for the details of the process, the wafer is inserted into a lateral oxidation furnace at 800°C for 8 minutes with oxygen flows, and a 3 nm oxide grows at the open areas between the lattices.

6.2 MOSFENS Spin Lattice Devices Characterization

The MOSFENS spin lattice devices were fabricated by using the nanostructure last design. Transistors in specific dies were patterned with a lattice array of 20 nm holes and 50 nm in period by EBL. If nano-LOCOS process works towards its design purpose, the

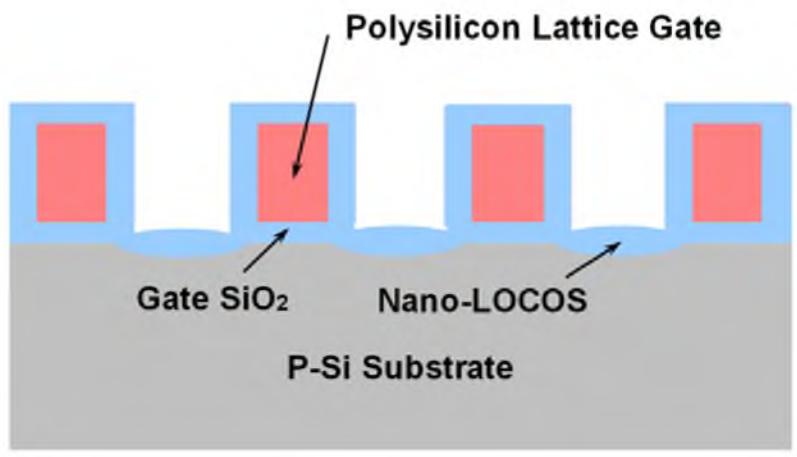

Fig. 6.5: The nanostructure last lattice formation: the nano-LOCOS

channel current should be lower on MOSFENS devices compared to those on standard MOSFETs due to the electron scattering effect from the undulating Si-SiO_2 interface. The V_g-I_{ds} (Fig. 6.6), V_{ds}-I_{ds} (Fig. 6.7) were measured for those MOSFENS spin lattice devices and the standard MOSFETs located in the same die. As expected, the room temperature current-voltage characteristics of MOSFENS spin lattice devices showed significantly reduced channel mobility, and the channel currents of those devices are about 15% of those of the standard MOSFETs in the same die.

The two-dimensional inversion layer electron concentration ns at the gate voltage V_g are given by the following expression [2]:

$$n_s = \frac{V_{th} N_a}{E_s} e^{\frac{(V_g - V_t)}{m V_{th}}} \tag{6.1}$$

where V_{th} is the thermal voltage, and $V_{th} = kT/q$, with k the Boltzmann constant. N_a is the substrate doping concentration and the gate threshold voltage V_t is around 0.25V.

E_s is the surface electric field, which can be calculated by:

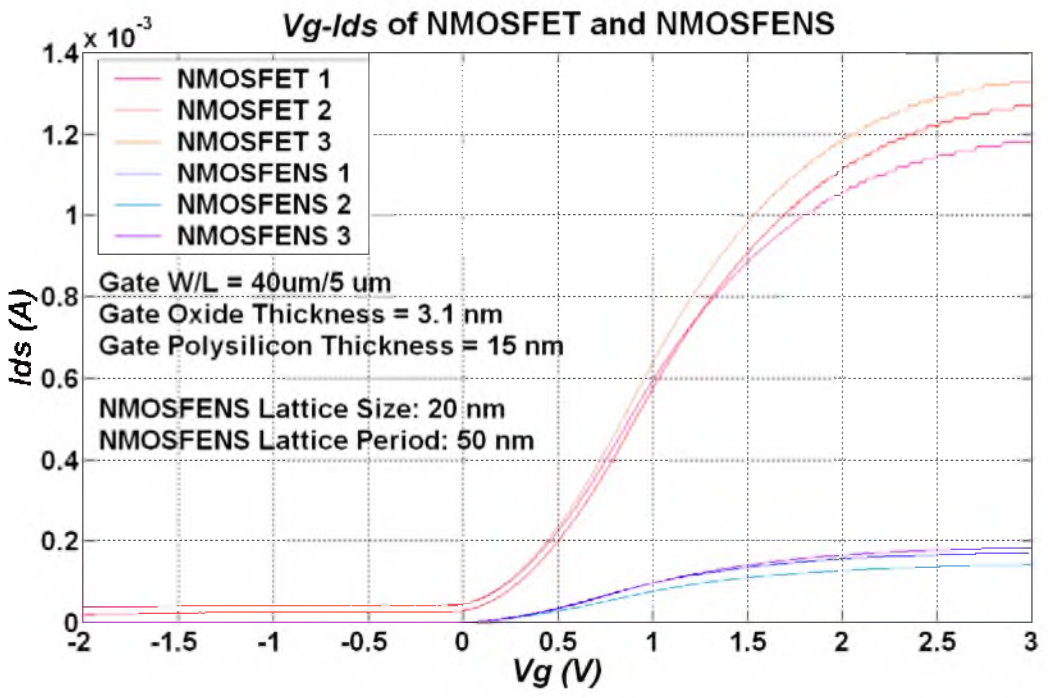

Fig. 6.6: V_g-I_{ds} of standard MOSFETs and MOSFENS spin lattice devices

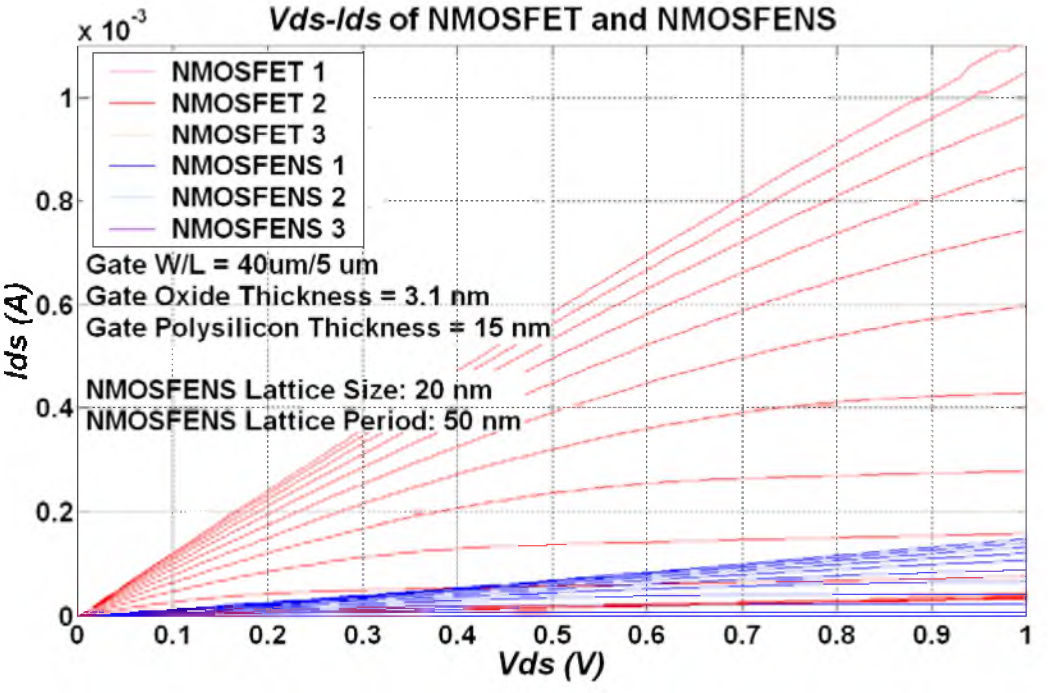

Fig. 6.7: V_{ds}-I_{ds} of standard MOSFETs and MOSFENS spin lattice devices

$$E_s = \sqrt{\frac{2qN_a(2\psi_B + V_{bs})}{\varepsilon_{Si}}} \tag{6.2}$$

where ψ_B is the difference between Fermi level and intrinsic level. And $\psi_B = V_{th}ln(N_a/n_i)$, where n_i is the intrinsic density.

The body-effect coefficient is m, which can be estimated from:

$$m = 1 + \frac{\sqrt{\varepsilon_{Si} qN_a /(4\psi_B)}}{C_{ox}} \tag{6.3}$$

where C_{ox} is the oxide capacitance per area, and $C_{ox} = \varepsilon_{ox}/t_{ox}$, with ε_{ox} and t_{ox} the oxide permittivity and the oxide thickness.

For those MOSFENS devices with lattice period l = 50 nm and hole size d = 20 nm, the electron-per-site filling factor v can be obtained by:

$$v = n_s(l^2 - \pi\left(\frac{d}{2}\right)^2) \tag{6.4}$$

The values of V_g corresponding to the different numbers of v is calculated and listed in Table 6.1. According to Mattis's prediction [1], and Miller's single band calculation [2] for a spin lattice array of 20 nm hole size and 50 nm period, at $v \approx 1.25$, the superconductivity phenomena may appear at a temperature scale around 9K. Fig. 6.8 depicts the average V_{ds}-I_{ds} of MOSFENS device with V_t = 0.25V. For a better visualization, the enclosed red box area is enlarged in Fig. 6.9 with different electron-per-site filling factor v denoted along with the predicted magnetic phases. Fig. 6.10 plots the correspondence between the gate voltage V_g and the electron-per-site filling factor v.

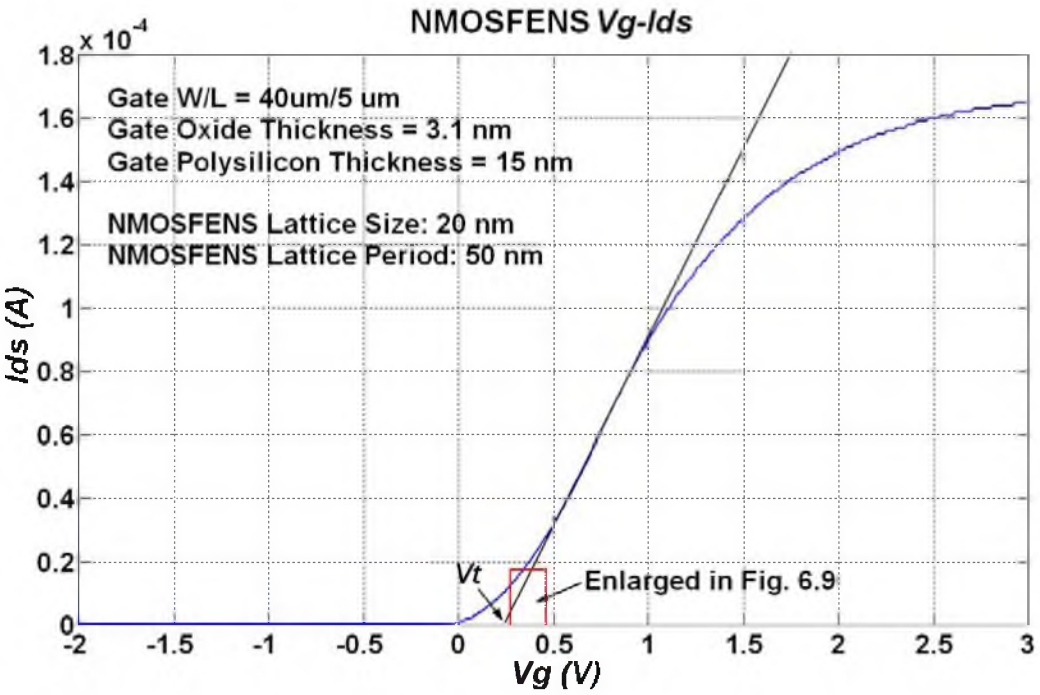

Fig. 6.8: Average V_{ds}-I_{ds} of MOSFENS spin lattice devices V_t = 0.25 V

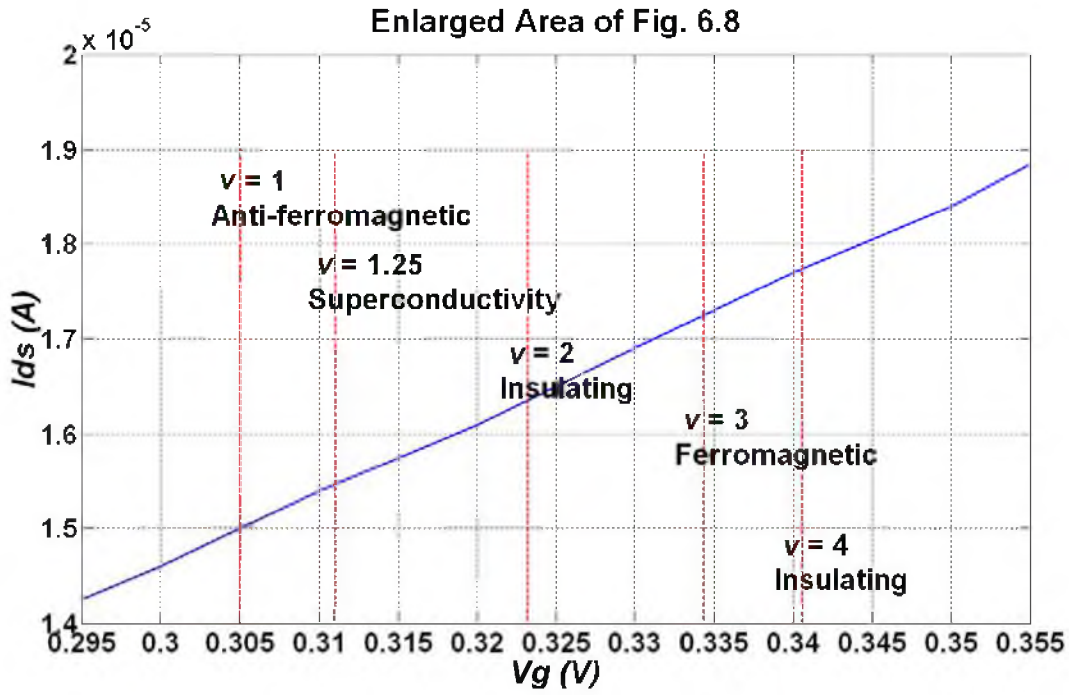

Fig. 6.9: Enlarged area of Fig. 6.8 with electron-per-site filling factor v denoted

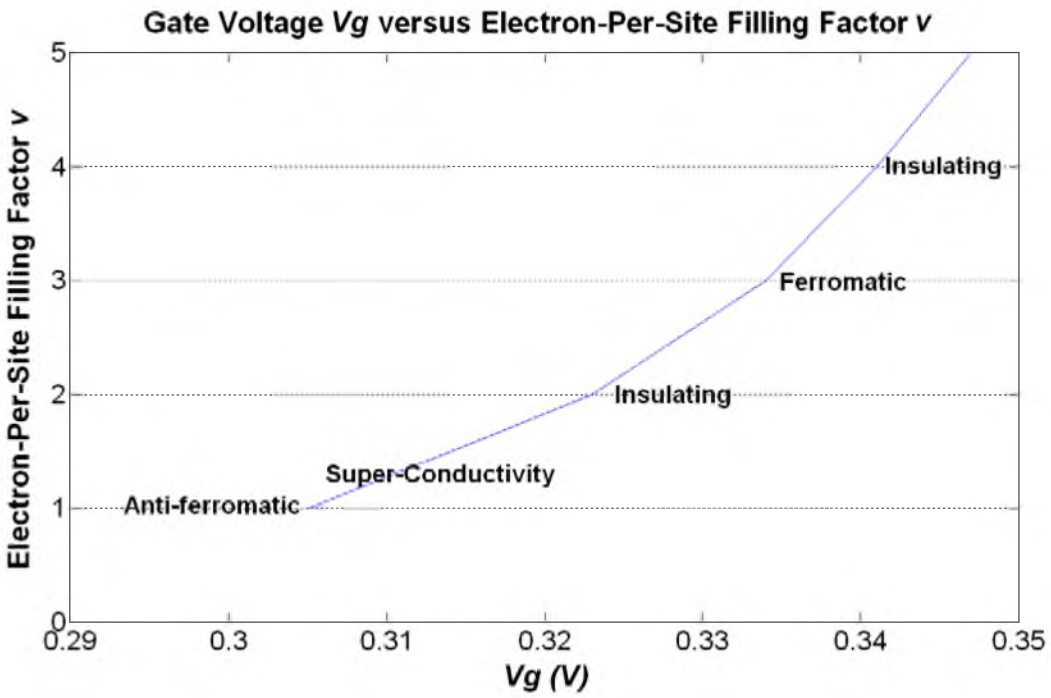

Fig. 6.10: The gate voltage V_g versus the electron-per-site filling factor v

Table 6.1: The gate voltage V_g at different electron-per-site filling factors v

Electron-per-site v	Electron Concentration n_s (cm^{-2})	Gate Voltage V_g (V)
1	4.57×10^{10}	0.305
1.25	5.72×10^{10}	0.311
2	9.15×10^{10}	0.323
3	1.37×10^{11}	0.334
4	1.283×10^{11}	0.341

6.3 Conclusions

MONSFEN spin lattice devices using the nanostructure last and the window isolation were successfully fabricated and characterized. The room temperature current-voltage characteristics of these devices show that the lattice nanostructures significantly reduce the average channel mobility. The results indicate that the nano-LOCOS process, which was invented for this work, is in agreement with its design purpose to provide a practical route to engineer and manipulate the in-plane electrons profile. The values of the gate voltage V_g corresponding to different electron-per-site filling factor v were calculated, which will be used to verify the future low temperature measurements of magnetic phases and superconductivity properties.

CHAPTER 7

SUMMARY AND RECOMMENDATIONS

7.1 Summary

In this work, the fabrication process of MOSFENS spin lattice devices were developed and integrated by combining a standard NMOS process and the gate stack processes was developed to meet the interface patterning requirements. By changing the gate potential of a MOSFENS spin lattice device, the electron occupation per site v can be varied, and the devices are predicted to show various magnetic behaviors and superconductivity properties.

Chapter 1 introduced the concept of the spin lattice along with its predicted magnetic and super conducting properties. It outlined the proposal of using silicon based MOS structures to realize the spin lattice, and thereafter the engineering challenges were laid out.

In Chapter 2, more theoretical details were given to explain why silicon is a good material selection for spin lattice applications. The optimal dimension scale was calculated by using a MOS model with the consideration that the fixed oxide charges should be significantly less than the electrons tied to spin lattice sites at the Si-SiO_2 interface.

Chapter 3 presented the nano-LOCOS process, which is designed to create an undulating Si-SiO_2 interface to confine the electrons to the sites, and it provided a

practical route to engineer and manipulate the in-plane electron profile. Options with different timing in nanostructures formation, either before or after the polysilicon gate patterning were introduced. In addition, two different isolation approaches, the window isolation and the mesa isolation, were discussed and compared.

In Chapter 4, a working NMOS process was described along with the successful characterization results. The MOSFETs fabricated were featured with a 3 nm gate oxide, and a 15 nm polysilicon gate.

In Chapter 5, as of the central MOSFENS spin lattices engineering challenges, the development work for MOSFENS lattice formation including the thin oxidation, EBL, the polysilicon RIE and CMP processes were introduced.

In Chapter 6, with the combination of the work from chapters 4 and 5, MOSFENS spin lattice devices with their polysilicon gates patterned with a lattice array of 20 nm holes and 50 nm in period by EBL were fabricated and characterized.

7.2 Conclusions

The transistors fabricated by using a NMOS process are in agreement with the MOSFENS design requirements. The characterizations show successful results, and this lays out the foundation for the next step in MOSFENS device fabrication.

With the success in developing the nano-LOCOS, the polysilicon RIE and EBL processes, the path was established to fabricate MOSFENS spin lattice devices by utilizing those processes to pattern the spin lattices on the polysilicon gates of MOSFETs.

The room temperature current-voltage characteristics of MOSFENS spin lattice devices show that the lattice nanostructures significantly reduce the average channel mobility as expected. However, the essentially unchanged threshold voltage indicates that

the nano-LOCOS process has given a low defect nanostructure interface. At room temperature, a change in gate potential of approximately of 18 mV changes the lattice electron occupation from v = 1 to v = 2. For these devices, the predicted temperature scale for superconductivity is approximately at 9 K. MOSFENS spin lattice devices are expected to show various magnetic behaviors and superconductivity at different electron-per-site filling factor v, which is modulated by the gate voltage V_g. This will be tested and verified in the future low temperature conductivity measurements.

This work demonstrates that by combining a standard NMOS process and the gate stack processes developed to meet the interface patterning requirements for spin lattices, silicon-based MOSFENS spin lattice devices can be successfully fabricated. This work has provided a platform, which will be used to verify and compare existing spin lattice theories and used as the guideline for spin lattices study and research in the future. Processes developed in this work make it possible to realize spin lattices on silicon based MOSFENS devices by using standard semiconductor fabrication equipments along with gate lattices fine patterning by EBL.

7.3 Future Work and Recommendations

For the next step of the research, we will continue characterization and optimization on MOSFENS designs and processes. Meanwhile, we will perform low temperature measurement for ferromagnetic, anti-ferromagnetic and insulating phases by measuring the conductivities of the spin lattices as functions of the gate potential, which will vary the electron occupation. Measurements will be made with standard lock-in amplifier techniques. The temperature-dependence will be measured to be below 10 K with a closed cycle helium refrigerator, and measurements will also be taken at 4.2 K and 1 K in

a helium-4 cryostat. The magnetic field dependence will also be measured, initially to a magnetic field strength of 0.5 T.

New processes for next generation MOSFENS development are proposed below.

7.3.1 HBr Polysilicon RIE

Recently, mixtures of HBr and Cl_2 gases have become an industry favorite for polysilicon etching. Bromine appears to be more successful than chlorine in reacting with etch by-products to form a passivating film on the masking photoresist, the underlying oxide, and the emerging sidewalls. The selectivity between the polysilicon and the oxide can easily be >100 and a small amount of additional of oxygen appears to improve etching anisotropy further [47, 48, 49]. There are a few publications about using HBr and helium combination to achieve an anisotropic and high selectivity polysilicon RIE etching process [50, 51].

7.3.2 Repeating Electron Beam Lithography to Achieve Small Period

While it was demonstrated that the EBL system is capable of extreme small features close to 10 nm, so far it has been difficult to achieve 20 nm period consistently to meet the requirement of MOSFENS. An idea of realizing 20 nm period by repeating EBL at an achievable 60 nm period is presented in Fig. 7.1.

7.3.3 Nitride ALD Deposition for SiN/SiO_2 Gate Stack

MOSFETs with a 2 nm silicon nitride and a 2 nm silicon dioxide sandwich structure gate stack were tested and they show superior gate to drain isolation compared to the

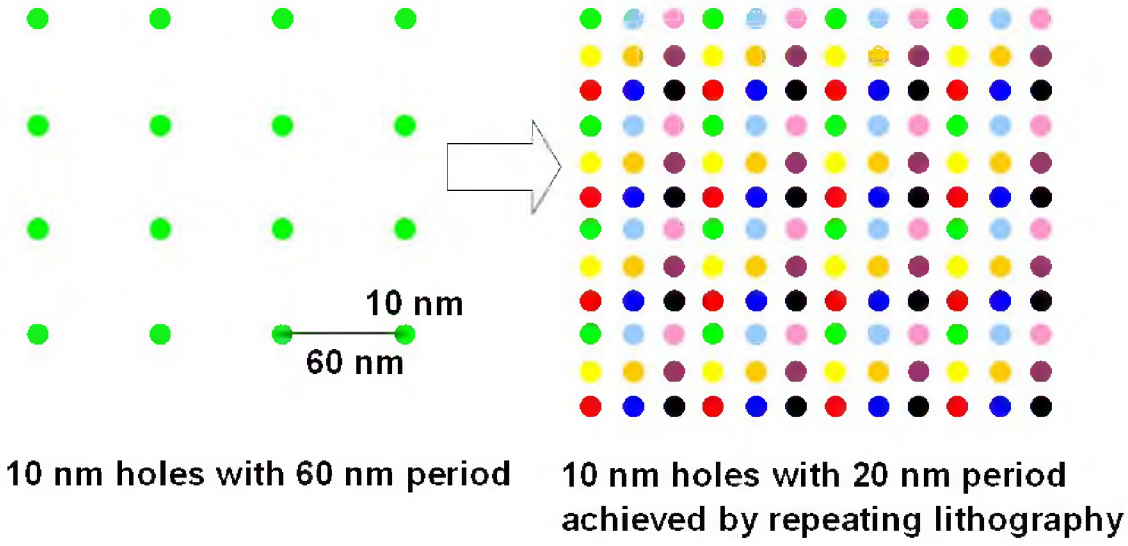

Fig. 7.1: Achieving 20 nm period by repeating EBL of 60 nm period

oxide only gate. It is known that the direct tunneling increases exponentially with decreasing dielectric thickness, and higher k materials are able to reduce the direct tunneling current and maintain the same drive-current capability. The purpose of using 2 nm oxide between the nitride and the silicon substrate is because the oxide is compatible with the silicon and it could preserve the critical high quality characteristics of the Si-SiO_2 interface. The minimum deposition rate in a lateral LPCVD furnace is 2 nm per minute, which makes the 2 nm nitride deposition too short to be controlled. As an alternative, ALD (atomic layer deposition) is the ideal candidate to accomplish this purpose.

ALD has several advantages over traditional CVD (Chemical Vapor Deposition) techniques. Firstly, it can be carried out at low temperature, typically < 400. Secondly, it uses a wider range of precursors. Thirdly, it produces very thin films. Finally, it inherently obtains 100% step coverage and excellent conformality even over the most

challenging topography, and with lower impurity levels. By definition, the thickness of each cycle can not exceed a few angstroms as determined by the lattice constant of the materials. The thickness of these films can be controlled simply by counting the cycles. The composition can also be modified and controlled at the atomic level; thus providing an opportunity to create new dielectrics that cannot be easily obtained by conventional means.

APPENDIX A

SI-SiO_2 INTERFACE CHARGES

AND TRAPS

As stated above, it is essential to control the concentration of the Si-SiO_2 interface charges and traps well below one electron per lattice site. Hence, it is important to understand the origin, mechanism of those charges and traps, and the methods to minimize them. The interface between Si and SiO_2 contain both charges and traps, and they have profound effects on the properties of the devices fabricated in the underlying silicon. There are four types of charges associated with the oxide and interface (Fig. A.1):

1. Fixed oxide charge, Q_f.

2. Mobile ionic charge, Q_m.

3. Interface trap charge, Q_{it}.

4. Oxide trapped charge, Q_{ot}. [52]

Fixed oxide charge, Q_f, is usually positive, and its polarity does not vary with the surface potential, and hence it is termed fixed charge. The fixed oxide charges reside as a thin sheet of charge near the Si/SiO_2 interface and commonly result from the structural changes associated with the transition region between Si and the oxide. In ultra-thin oxides (<3.0 nm) the charges are closer to the interface or distributed through the oxide. It has been experimentally demonstrated that the value of Q_f depends on several factors:

1. The silicon crystal orientation;

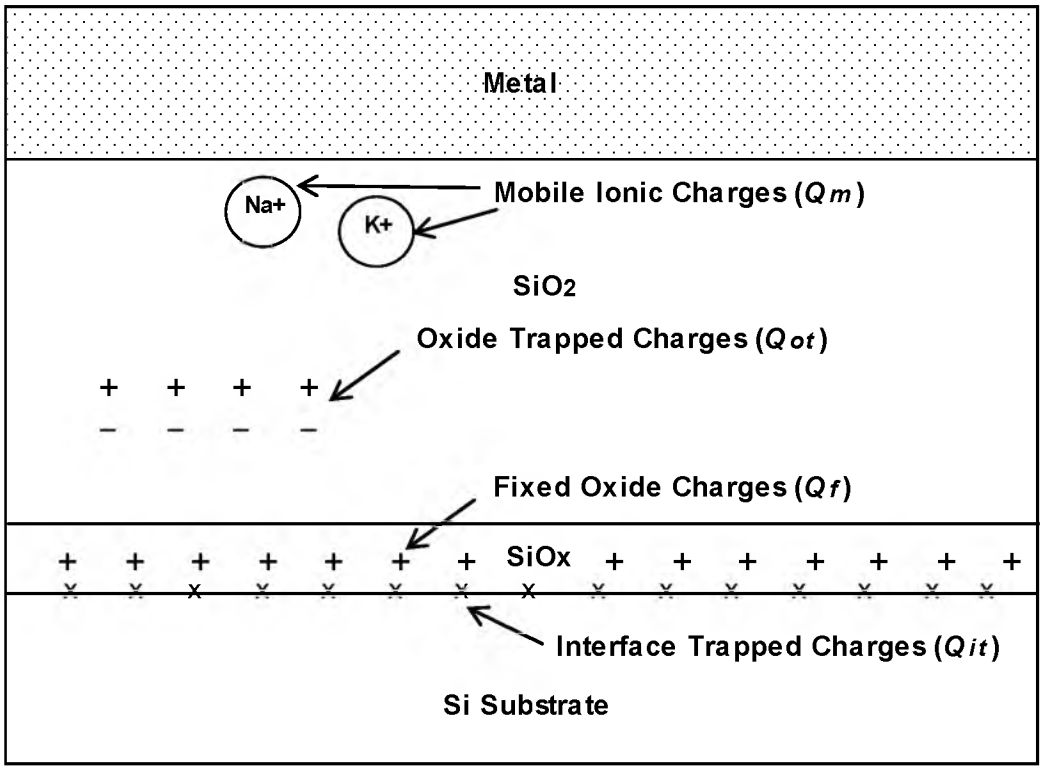

Fig. A.1: The Si-SiO_2 interface charges

2. The oxidation temperature and ambient;

3. The post-oxidation anneal conditions.

The lowest values of N_f are obtained for oxidation or anneal at the highest temperatures [53]. POA is generally carried out in a nitrogen ambient in the furnace, and it is often performed at a higher temperature than the oxidation temperature [54].

Mobile ionic charge, Q_m, is commonly caused by the presence of ionized alkali metal atoms like Na^+, K^+. These ions have very high diffusivity in oxide film, and they can drift through thin oxide even at room temperature when a positive bias is applied to the gate electrode. The drift of the mobile ion charges from the gate electrode to the silicon interface can result in MOSFET threshold voltage shift. The amount of mobile ion charges incorporated into the oxide depends on the cleanliness of the oxidation process.

Interface trap charge, Qit, refers to a charge that is localized at sites near the Si/SiO_2 interface. D_{it}, the interface trap density per unit energy is defined to characterize those interface states. It suggests that the interface trap charges arise from unsatisfied chemical bonds at the interface, called dangling bonds. The presence of a large amount of interface trap charges can significantly reduce the channel mobility of the transistor and thereby degrade the device performance. *Dit* tends to decrease as the oxidation temperature increases, but annealing in an inert gas does not further reduce *Dit*. The level of *Dit* can be reduced to an acceptable level (3 to 5 $\times$ $10^{10}/cm^2eV$) by applying a PMA (post-metallization annealing). The PMA is performed after the device has been metalized with the aluminum interconnection, and it is carried out in a hydrogen forming gas in the temperature range of 400 to 450°C for 5 to 30 minutes. It is believed that atomic hydrogen is formed in the presence of aluminum, and the atomic H diffuses to the Si/SiO_2 interface where it reacts with dangling bonds, passivating the bonds and reducing the interface trap charges [55].

Oxide trapped charges, Q_{ot}, are located in the bulk of the oxide, but are neutral until they interact with injected carriers and trap them. As a result, the traps can become charged either positive or negative depending on whether they trap holes or electrons. The oxide trapped charges are generally associated with defects in the oxide. Device failures caused by oxide trapped charges are either threshold voltage V_t drift outside the operating range or premature and catastrophic dielectric breakdown. The density of oxide trapped charges can be significantly reduced with an appropriate POA process [56].

In MOSFENS process, pre-gate oxidation cleaning, POA and PMA processes are used to reduce the interface charges and traps.

APPENDIX B

LITHOGRAPHY PROCESS

B.1 Negative Photoresist

A negative i-line photoresist AZnLOF 2020 is applied, and the wafer is spun with 1000 RPM acceleration for 5 seconds, then 3000 RPM for 45 seconds on the Solitec 5100 resist coating system. Then the wafer is soft-baked on a hotplate at 110°C for 1 minute. The wafer is aligned to the mask, and is exposed for 6.5 seconds at a dose of 120 mJ/cm^2 on the EV420, a contact mask-aligner. After the exposure, the wafer is hard-baked on the hotplate at 110°C for 1 minute. Different than positive photoresist, hard-bake for AZnLOF 2020 negative photoresist takes place before the development. Other than harden photoresist, it mainly promotes the cross-link photo-chemical transformations. After the hard baking, the wafer is developed in TMAH (tetramethylammonium hydroxide) based developer AZ300 at room temperature for 45 seconds.

B.2 Positive Photoresist

A positive photoresist Shipley Microposit s1813 is applied to the wafer, then the wafer is spun with 1000 RPM acceleration for 5 seconds, then 3000 RPM for 45 seconds. The wafer is soft-baked on the hotplate at 95°C for 4 minutes, then it is aligned to the mask on the EV420 system and is exposed for 6.5 seconds at a dose of 120 mJ/cm^2. For the mask with a small feature size like mask two, the exposure time is 2.5 seconds.

Following the exposure, the wafer is developed in AZ300 at room temperature for 25 seconds, then finally the wafer is hard-baked on the hotplate at 125°C for 4 minutes.

APPENDIX C

NANOSTRUCTURE FIRST PROCESS

The process of the nanostructure first is introduced below, and it does not require the thin polysilicon deposition and the polysilicon RIE. The process steps of the nanostructure first are the same as the ones of nanostructure last till the gate oxidation, and the steps after the gate oxidation are described. The process adopts an idea similar to standard LOCOS process, but it is implemented on a much smaller nanometers scale.

Step 1 is nitride deposition. After the thin gate oxidation, a thin silicon nitride layer is deposited on the top. The nitride will be used as the selective masking layer in the nano-LOCOS process later. The nitride is grown in a lateral LPCVD furnace and the process uses dichlorosilane ($SiCl_2H_2$, DCS) and ammonia (NH_3) at a temperature of 780°C. The flow-rate of DCS and NH_3 is set at 20 sccm and 80 sccm, respectively and the deposition rate is approximately 4 nm per minute.

Step 2 is nitride RIE. After the nitride deposition, the future gate areas are firstly patterned. A nitride RIE process with high etching rate is used for this step. At 200 W power, 1.5 Torr. pressure, 0.8 cm gap distance and helium 120 sccm/CHF_3 30 sccm/CF_4 90 sccm, the etching rate is about 115 nm per minute. The sidewall profile is about 70 degrees. Subsequently EBL is used to pattern an array of lattices on the gate areas (Fig. C.1). This time, a nitride RIE process with much lower etching rate is used. At 200 W power, 0.5 Torr pressure, 0.8cm gap distance, helium 120 sccm/CHF3 30 sccm/CF4 90

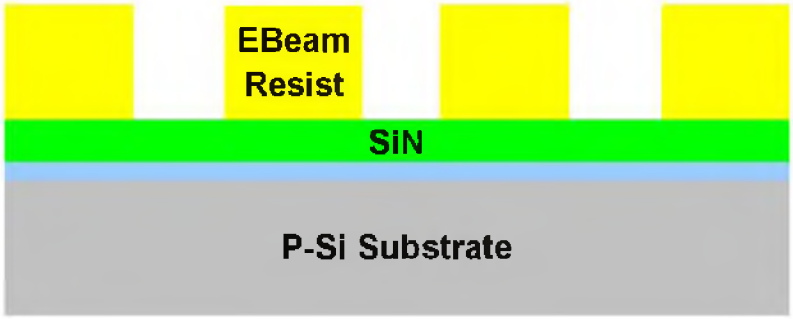

Fig. C.1: The nanostructure first lattices formation: nitride deposition

sccm, the etching rate is about 1.2 to 1.9 nm per minute. The selectivity to the gate oxide is about 1. At this step, it is okay to totally or partially remove the 3 nm gate oxide underneath. Fig. C.2 shows a cross-section view after nitride RIE.

Step 3 is DHF etching. The wafer is dipped in 1:104 DHF at room temperature for 3 minutes to remove the oxide at the open holes after the nitride RIE.

Step 4 is nano-LOCOS. After PMMA resist is stripped, the nano-LOCOS oxidation is carried out to grow a 3 nm oxide at the open holes, which have no nitride coverage (Fig. C.3).

Step 5 is nitride wet etching. The nitride will be removed in hot 85% phosphorous acid at 160°C. The etching rate is 6.5 nm per minute with the etching rate on the oxide around 0.2 nm per minute. Fig. C.4 shows a cross-section view after nitride wet etching.

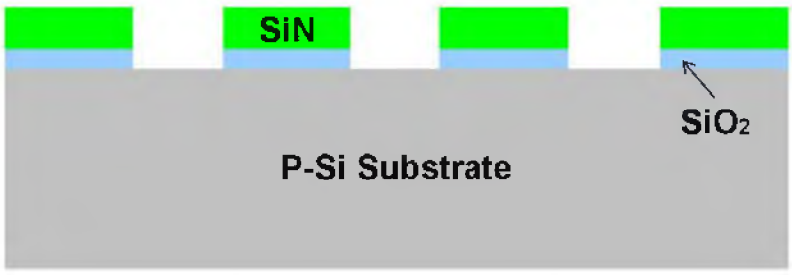

Fig. C.2: The nanostructure first lattices formation: nitride RIE

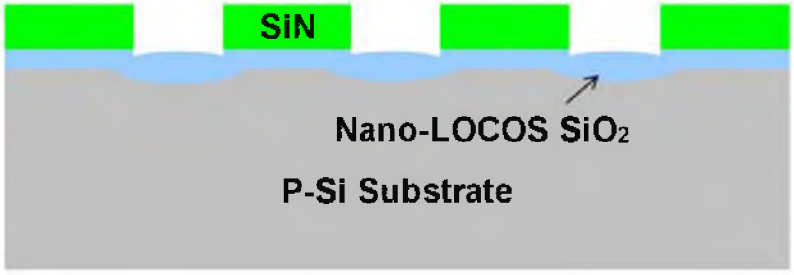

Fig. C.3: The nanostructure first lattices formation: nano-LOCOS

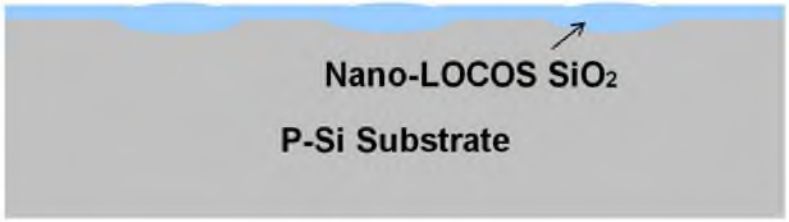

Fig. C.4: The nanostructure first lattices formation: nitride wet etching

The etch rate of the silicon nitride varies with the temperature and the concentration of phosphorous acid. Since the bath is operated at high temperature, water readily evaporates from the solution and the concentration of phosphorous acid changes. Therefore, it is necessary to control the concentration of phosphorous acid as well as the temperature of the bath. The wet bench at the Nanofab is not equipped with high temperature heating and an automatic concentration control function. At the implementation, phosphorous acid is heated by a hot plate in a glass beaker to 160°C, with an aluminum foil seal the top of the beaker to prevent the water from evaporating. The wafer is preheated on another hot plate at 150°C before it is dipped in hot phosphorous acid. This way, the chemical will not be cooled down due to heat exchange with the wafer. According to Geldger and Hauser's study [57], the etching is significant

only when the temperature is above 140°C, and the etching rate to the oxide underneath is minimum. So once the nitride is cleared, the beaker along with the wafer and phosphorous acid are placed into a room temperature water tank. The temperature of the phosphorous acid quickly drops below 140°C when the etching is ceased.

Step 6 is polysilicon deposition. After the nitride is removed, a polysilicon film is deposited on the top of the oxide (Fig. C.5).

Step 7 is polysilicon gate patterning. The polysilicon will be patterned into the gate features at this step.

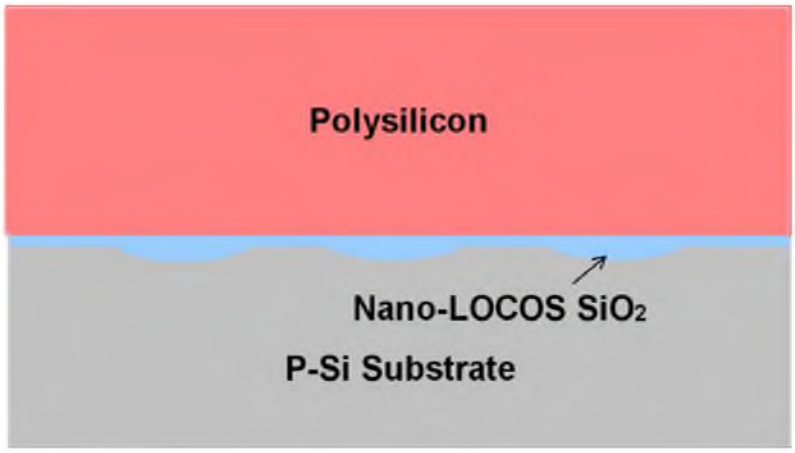

Fig. C.5: The nanostructure first lattices formation: polysilicon deposition

APPENDIX D

NANOSTRUCTURE LAST WINDOW

PROCESS FLOW

No.	Step	Equipment	Details	Target
1	Wafer Start	N/A	P type <100> substrate	
2	Field Oxidation Growth	Canary Oxidation Furnace	1000°C, O_2 2.25 slpm/ H_2 4 slpm, 70 minutes	370 nm
3	Photoresist Coating	Solitec 5110	AZnLOF 2020, 3000 RPM, 55 seconds	
4	Soft-Bake	Hot Plate	110°C, 1 minute	
5	Mask 1 Exposure	EV420 Aligner	120 mJ/cm^2, 6.5 seconds	
6	Hard-Bake	Hot Plate	110°C, 1 minute	
7	Development	Wet Bench	AZ300, 45 seconds	
8	BOE Etching	Wet Bench	1:6 BOE, R.T., 6 minutes	
9	Photoresist Strip	Wet Bench	Acetone then IPA	
10	DHF Etching	Wet Bench	1:104 DHF, R.T., 3 min	
11	Gate Oxide Growth	Canary Oxidation Furnace	800°C, O2 3.5 slpm, 8 minutes	3 nm
12	Post-Oxidation Annealing	Canary Oxidation Furnace	In-situ, 1050°C, N_2 1 slpm, 10 minutes	
13	Gate Polysilicon Deposition	Canary LPCVD Furnace	630°C, SiH_4 20 sccm, 160 mTorr, 9 minutes	40 nm
14	Photoresist Coating	Solitec 5110	Shipley 1813, 3000RPM, 45 seconds	
15	Soft-Bake	Hot Plate	95°C, 4 minute	

No.	Step	Equipment	Details	Target
16	Mask 2 Exposure	EV420 Aligner	120 mJ/cm^2, 2.5 seconds	
17	Development	Wet Bench	AZ300, 25 seconds	
18	Hard-Bake	Hot Plate	125°C, 4 minute	
19	DHF Etching	Wet Bench	1:104 DHF, R.T., 3 min	
20	Polysilicon RIE	LAM490	Cl_2/He 80/120 sccm, 200 W, Gap 1.5 cm, 3 minutes	
21	Photoresist Strip	Wet Bench	Acetone then IPA	
22	DHF Etching	Wet Bench	1:104 DHF, R.T., 1 min	
23	Phosphorous Diffusion	Canary Diffusion Furnace	1000°C, N_2 1 slpm, 20 min	
24	DHF Etching	Wet Bench	1:104 DHF, R.T., 3 min	
25	PMMA Coating	Spinner	100 nm, Aldrich 996000 molecular weight	
26	Soft-Bake	Hot Plate	100°C, 30 minute	
27	Electron Beam Lithography	FEI Nova NanoSEM 630	30 kV, 20 pA, 2 fC dose	
28	Development	Wet Bench	1:3 4-methyl-2-pentanone/IPA, 70 seconds	
29	Hard-Bake	Hot Plate	105°C, 70 minute	
30	DHF Etching	Wet Bench	1:104 DHF, R.T., 2 min	
31	Spin Lattice Poysilicon RIE	LAM490	Cl_2/He 80/120 sccm, 200 W, Gap 1.5 cm, 3 minutes	
32	PMMA Strip	Wet Bench	Acetone then IPA	
33	Nano-LOCOS Oxidation	Canary Oxidation Furnace	800°C, O_2 3.5 slpm, 8 minutes	3 nm
34	Post-Oxidation Annealing	Canary Oxidation Furnace	In-situ, 1050°C, N_2 1 slpm, 10 minutes	
35	SOG Coating	Solitec 5110	Honeywell Accuglass, 2000 RPM, 40 seconds	
36	Soft-Bake	Hot Plate	125°C, 3 minute	
37	Hard Bake	Lindberg Blue Oven	400°C, N_2 1 slpm, 60 minutes	

No.	Step	Equipment	Details	Target
38	Photoresist Coating	Solitec 5110	Shipley 1813, 3000RPM, 45 seconds	
39	Soft-Bake	Hot Plate	95°C, 4 minute	
40	Mask 3 Exposure	EV420 Aligner	120 mJ/cm^2, 6.5 seconds	
41	Development	Wet Bench	Shipley 352, 30 seconds	
42	Hard-Bake	Hot Plate	125°C, 4 minute	
43	BOE Etching	Wet Bench	1:6 BOE, R.T., 4.5 minutes	
44	Photoresist Strip	Wet Bench	Acetone then IPA	
45	Photoresist Coating	Solitec 5110	Shipley 1813, 3000RPM, 45 seconds	
46	Soft-Bake	Hot Plate	95°C, 4 minute	
47	Mask 4 Exposure	EV420 Aligner	120 mJ/cm^2, 6.5 seconds	
48	Development	Wet Bench	Shipley 352, 30 seconds	
49	Hard-Bake	Hot Plate	125°C, 4 minute	
50	BOE Etching	Wet Bench	1:6 BOE, R.T., 5.5 minutes	
51	Photoresist Strip	Wet Bench	Acetone then IPA	
52	DHF Etching	Wet Bench	1:104 DHF, R.T., 3 min	
53	Aluminum Sputtering	Denton Sputter	Al/0.5% Si target, Ar 80 sccm, 100 W, 2×10^{-6} Torr, 25 minutes	500 nm
54	Photoresist Coating	Solitec 5110	Shipley 1813, 3000RPM, 45 seconds	
55	Mask 5 Exposure	EV420 Aligner	120 mJ/cm^2, 6.5 seconds	
56	Development	Wet Bench	Shipley 352, 30 seconds	
57	Hard-Bake	Hot Plate	125°C, 4 minute	
58	Aluminum Etching	Wet Bench	Al etchant, R.T., 5 minutes	
59	Photoresist Strip	Wet Bench	Acetone then IPA	
60	Contact Annealing	Lindberg Furnace	400°C, Ar/H_2 1 slpm, 40 minutes	

REFERENCES

[1] D.C. Mattis, "Design of a Nanomagnet," *Journal of Statistical Physics*, vol. 116, no. 1-4, pp 773-782, 2004.

[2] M. Miller, "Silicon Field-Effect Spin Lattices for Magnetism and Superconductivity Tests," unpublished, 2013.

[3] A. Sugimura, "Possibility of Magnetic Ordered States in Semiconductor Quantum Dot System," *Japanese Journal of Applied Physics*, vol. 29, no. part 2, no. 12, pp. L2463-2465, 1990.

[4] T. Ando, A.B. Fowler, and F. Stern, "Electronic Properties of Two-Dimensional Systems," *Rev. Mod. Phys.*, vol. 54, no. 2, pp. 437-672, 1982.

[5] J. Yang, M. Miller et.al., "Fabrication Process Development for Metal-Oxide-Semiconductor Field-Effect Nanostructure Spin Lattice Devices," unpublished, 2013.

[6] E. Lieb, "Two Theorems on the Hubbard Model," *Phys. Rev. Lett.*, vol. 62, pp. 1201–1204, 1989.

[7] M. Koskinen, S.M. Reimann, and M. Manninenn, "Spontaneous Magnetism of Quantum Dot Lattices," *Phys. Rev. Lett.*, vol. 90, 066802-1, 2003.

[8] C.S. Lent, P.D. Tougaw, and W. Porod, "Bistable Saturation in Coupled Quantum Dots for Quantum Cellular Automata," *Appl. Phys. Lett.*, vol. 62, pp. 714-716, 1993.

[9] E. Manousakis, "A Quantum-Dot Array as Model for Copper-Oxide Superconductors: A Dedicated Quantum Simulator for the Many-Fermion Problem," *Journal of Low Temperature Physics*, vol. 126, no. 5, pp. 1501-1513, 2002.

[10] D. Mattis, "Magnetism and Superconductivity in Nanoarchitectures," *Physica B: Condensed Matter*, vol. 384, no. 1-2, pp. 239-243, 2006.

[11] T. Kimura, H. Tamura, K. Kuroki, K. Shiraishi, H. Takayanagi, and R. Arita, "Superconductivity in Quantum Dot Superlattices Composed of Quantum Wire Networks,"*Phys. Rev. B*, vol. 66, no. 13, pp. 132508, 2002.

[12] P.W. Anderson, *The Theory of Superconductivity in the High-T_c Cuprate Superconductors.* [On-line]. Available: press.princeton.edu [1997].

[13] M. Fujita, T. Umeda, and M. Yoshida, "Polymorphism of Carbon Forms: Polyhedral Morphology and Electronic Structures," *Phys. Rev.B,* vol. 51, pp. 13778, 1995.

[14] M. Fujita, K. Wakabayashi, K. Nakada and K. Kusakabe, "Peculiar Localized State at Zigzag Graphite Edge," *J. Phys. Soc. Jpn.*, vol. 65, pp. 1920, 1996.

[15] K. Kusakabe, K. Wakabayashi, M. Igami, K. Nakada, M. Fujita, "Magnetism of Nanometer-Scale Graphite with Edge or Topological Defects," *Mol. Cryst. Liq. Cryst.*, vol. 305, pp. 445, 1997.

[16] A. Yajima, M. Tsukada, S. Watanabe, M. Ichimura, Y. Suwa, T. Onogi and T. Hashizume, "First-Principles Calculation of As Atomic Wires on a H-Terminated Si (100) Surface," *Phys. Rev. B*, vol. 60, pp. 1456, 1999.

[17] K. Kumakura, J. Motohisa, and T. Fukui, "Transport Characterization of GaAs Quantum Dots Connected with Quantum Wires Fabricated by Selective Area Metalorganic Vapor Phase Epitaxy," *Solid-State Electronics*, vol. 42, no. 7-8, pp. 1227-1231, 1998.

[18] P. Mohan, F. Nakajima, M. Akabori, J. Motohisa, and T. Fukui, "Fabrication of Semiconductor Kagome Lattice Structure by Selective Area Metalorganic Vapor Phase Epitaxy," *Appl. Phys. Let.*, vol. 83, no. 4, pp. 689-691, 2003.

[19] P. Mohan, J. Motohisa, and T. Fukui, "Realization of InAs-Based Two-Dimensional Artificial Lattice by Selective Area Metalorganic Vapor Phase Epitaxy," *Appl. Phys. Let*,vol. 84, no. 14, pp. 2664-2666, 2004.

[20] S. Okada and A. Oshiyama, "Nearly Free Electron States in Carbon Nanotube Bundles," *Phys. Rev. B*, vol. 62, pp. R13286, 2000.

[21] Y. Momiyama, et al., "Ultra-Thin Ta_2O_5/SiO_2 Gate Insulator with TiN Gate Technology for 0.1μm MOSFETs," *Dig. Symp. VLSI Tech.*, pp. 135-136, 1997.

[22] D.A. Buchanan, et al., "80 nm Polysilicon Gated n-FETs with Ultra-Thin Al_2O_3 Gate Dielectric for ULSI Applications," *Tech. Dig. IEDM*, pp. 223-226, 2000.

[23] W.J. Qi, et al., "MOSCAP and MOSFET Characteristics Using ZrO_2 Gate Dielectric Directly on Si," *Tech. Dig. IEDM*, pp. 145-148, 1999.

[24] C. Hobbs, et al., "80 nm Poly-Si Gate CMOS with HfO_2 Gate Dielectric," *Tech. Dig. IEDM*, pp. 651-654, 2001.

[25] R.A. Chapman, et al., "Sub-100 nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process," *Tech. Dig. IEDM*, pp. 821-824, 1997.

[26] M.E. Alperin, T.C. Hollaway, R.A. Haken, et al., "Development of the Self-Aligned

Titanium Silicide Process for VLSI Applications," *Solid-State Circuits, IEEE Journal of*, vol. 20, pp. 61-69, 1985.

[27] J.Y.C. Sun, et al., "Foundry Technology for the Next Decade," *Tech. Dig. IEDM*, pp. 321-324, 1998.

[28] M. Armstrong, et al., "A 90 nm High Volume Manufacturing Logic Technology Featureing Novel 45nm Gate Length Strained Silicon CMOS Transistors," *Tech. Dig. IEDM*,pp. 1161-1163, 2003.

[29] M.E. Peskin and H.D. Schroeder, *An introduction to quantum field theory*. Cambridge University Press, 1993.

[30] M.K. Wu, J.R. Ashburn, C.J. Torng, P.H. Hor, R.L. Meng, L. Gao, Z.J. Huang, Y.Q. Wang, and C.W. Chu, "Superconductivity at 93 K in a New Mixed-Phase Y-Ba-Cu-O Compound System at Ambient Pressure," *Phys. Rev. Lett.*, vol. 58 (9), pp. 908-910,1987.

[31] Y. Taur and T.H. Ning, *Fundamentals of modern VLSI devices, 2nd ed.* Cambridge University Press, 2009.

[32] D.K. Schroder and J.A. Babcock, "Negative Bias Temperature Instability: Road to Cross in Deep Submicron Silicon Semiconductor Manufacturing," *Journal of AppliedPhysics*, vol. 94, no. 1, pp. 1-18, 2003.

[33] J.A. Appels, E. Kooi, M.M. Paffen, et al., "Local Oxidation of Silicon and its Application in Semiconductor-Device Technology, " *Philips Research Reports*, vol. 25, no. 2, pp.118-132. Apr. 1970.

[34] N. Shima and H. Aoki, "Electronic Structure of Super-Honeycomb Systems: A Peculiar Realization of Semimetal/Semiconductor Classes and Ferromagnetism," *Phys. Rev. Lett.*, vol. 71, pp. 4389, 1993.

[35] T. Matsuzaka, Y. Soda, "Electron Beam Lithography System for Nanometer Fabrication" *Hitachi Review*, vol. 48, no.6, pp. 340-343, 1999.

[36] J.L. Vossen, et al., "Preparation of Surfaces for High Quality Interface Formation," *J. Vac. Sci Tech.*, vol. 2, pp. 212-215, 1984.

[37] H. Watanabe, K. Shimizu, Y. Takeuchi and S. Aritome "Corner-Rounded Shallow Trench Isolation Technology to Reduce the Stress-Induced Tunnel Oxide Leakage Current for Highly Reliable Flash Memories," *Electron Devices Meeting, IEDM*, pp. 833-836, 1996.

[38] R.B. Marcus and T.T. Sheng, "The Oxidation of Shaped Silicon Surface," *Extended Abstracts, Electrochem. Soc. Mtg.*, vol. 26, pp. 1278-1282, 1982.

[39] S.V. Nguyen, "High-Density Plasma Chemical Vapor Deposition of Silicon-Based Dielectric Films for Integrated Circuits," *IBM Journal of Research and Development*, vol. 43, pp. 109-126, 1999.

[40] A. Reisman, E.H. Nicollian, C.K. Williams and C.J. Men, "The Modelling of Silicon Oxidation from 1×10^{-5} to 20 Atmospheres," *J. Electron Materials*, vol. 16, pp. 45-55, 1987.

[41] E.A. Ray, J. Rozen, et al., "Pressure Dependence of SiO_2 Growth Kinetics and Electrical Properties," *J.of Appl. Phys.*, vol. 103, pp. 023522-023522-7, 2008.

[42] R.J. Archer, "Determination of the Properties of Films on Silicon by the Method of Ellipsometry," *J. of the Optical Soc. Of America*, vol. 52, pp. 970-977, 1962.

[43] C.J. Mogab, "Loading Effect in Plasma Etching," *J. Electrochem. Soc.*, vol. 124, pp. 1262-1268, 1977.

[44] M.S. Cher, et al., "Anisotropic Polysilicon Plasma Etch Using Fluorine Gases," US Patent 5453156, 1995.

[45] J. Olsen and F. Moghadam, "Planarization Techniques," in *Handbook of Metallization form Integrated Circuits*, Eds. S. R. Wilson, C.J. Tracy, and J.L. Freeman, Noyes Pubs. 1993.

[46] W.J. Patrick, et al., "Application of Chemical Mechanical Polshing to the Fabrication of VLSI Circuit Interconnections," *J. Electrochem. Soc.*, vol. 138, pp. 1778-1784,1991.

[47] M. Haverlag, G.S. Oehrlein, D. Vender, "Sidewall Passivation During the Etching of Poly-Si in an Electron Cyclotron Resonance Plasma of HBr," *J. Vac. Sci Tech.*, vol. 12, pp. 96-101, 1994.

[48] I. Tepermeister, D.E. Ibbotson, J.T.C. Lee, "Comparison of Advanced Plasma Sources for Etching Applications II Langmuir Probe Studies of a Helicon and a Multiple Electron Cyclotron Resonance Source," *J. Vac. Sci Tech.*, vol. 12, pp. 2322-2332, 1994.

[49] R. Kraft, T. Boonstra, S. Prengle, "Etching 0.35 μm Polysilicon Gates on a High-Density Helicon Etcher," *J. Vac. Sci Tech.*, vol. 14, pp. 543-546, 1996.

[50] M.C. Lemme, T. Mollehhauer, et al., "Highly Selective HBr Etch Process for Fabriccation of Triple-Gate Nano-Scale SOI-MOSFETs," *Microelectronic Engineering*, vol. 73-74, pp. 346-350, 2004.

[51] T. Wahlbrink, T. Mollenhauer, et al., "Highly Selective Etch Process for Silicon on

Insulator Nano-Devices," *Microelectronic Engineering*, vol. 78-79, pp. 212-217, 2004.

[52] B.E. Deal, "Standardized Terminology for Oxide Charges Associated with Thermally Oxidized Silicon," *IEEE Trans, Electron Dev.*, vol. 27, pp. 606-608, 1980.

[53] B.E. Deal, M. Sklar, A.S. Grove, and E.H. Snow, "Characteristics of the Surface State Charge of Thermally Oxidized Silicon," *J. Electronchem. Soc.*, vol. 114, pp. 266-274, 1967.

[54] F. Montillo and P. Balk, "High-Temperature Annealing of Oxidized Silicon Surfaces," *J. Electrochem. Soc.*, vol. 118, No. 9, pp. 1463-1468, 1971.

[55] Z. Chen, et al., "Deuterium Process of CMOS Devices: New Phenomenon and Dramatic Improvement," *Dig. Symp. VLSI Tech.*, pp. 180-181, 1998.

[56] T. Hori, *Gate Dielectrics and MOS ULSIs*. Springer-Verlag, Heidelberg, 1997.

[57] W. Van Geldger and V.E. Hauser, "The Etching of Silicon Nitride in Phosphoric Acid with Silicon Dioxide as a Mask," *J. Electrochem. Soc.*, vol. 114, pp. 869-872, 1967.